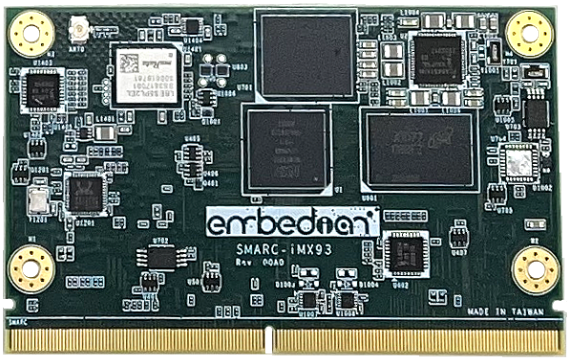
User's Manual

SMARC Computer on Module

NXP *i.MX93* 2 x Cortex-A55 up to 1.7GHz
ARM Cortex-M33 real-time Processor at 250Mhz
ARM Ethos™-U65 microNPU up to 0.5 TOPS
1 x 24bits single-channel LVDS LCD/MIPI-DSI x 4
4 x COM Ports
1 x SDHC
WiFi a/b/g/n/ac/ax + BT 5.3 (optional)
1 x USB OTG 2.0, 4 x USB Host 2.0
2 x 10/100/1000M Gigabit Ethernet with TSN
2 x CAN-FD, 2 x SPIs, 4 x I2Cs, 1 x MIPI_CSI and 2 x I2S

SMARC-iMX93

(SMARC 2.2 Specification Compliant)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SMARC-iMX93
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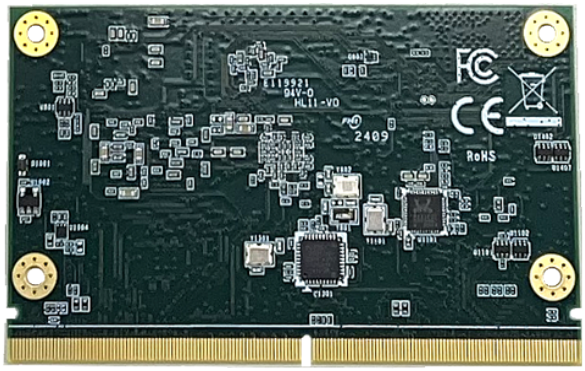
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Revision History

Revision	Date	Changes from Previous Revision
1.0	2024/ 10/01	Initial Release
		i.

USER INFORMATION

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Table of Contents

Using this Manual

This guide provides information about the Embedian *SMARC-iMX93* for NXP *i.MX93* embedded *SMARC* core module family.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This Convention	Is used for
Italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

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Additional Resources

Please also refer to the most recent *NXP i.MX93* processor reference manual and related documentation for additional information.

Introduction

This Chapter gives background information on the *SMARC-iMX93*
Section include：

- Features and Functionality
- Module Variant
- Differences between Module Variants
- Block diagram
- Software Support / Hardware Abstraction
- Module Variant
- Document and Standard References

Chapter 1 Introduction

The SMARC-iMX93 SMARC 2.2 module family is highly scalable and equipped with i.MX 93 Applications Processors manufactured by NXP. The processors integrate Arm Cortex-A55 cores, bringing performance and energy efficiency to Linux-based edge applications and the Arm Ethos-U65 microNPU, enabling developers to create more capable, cost-effective and energy-efficient machine learning (ML) applications. The i.MX 93 processors deliver advanced security with integrated EdgeLock secure enclave and an efficient pixel pipeline to perform 2D graphics processing to realize cost-effective GUI solutions.

The *SMARC-IMX93* provides fast and low power LPDDR4 memory technology with inline ECC support, combined with 16GB eMMC Flash memory. Various interfaces for embedded applications such as Dual Gigabit Ethernet, USB 2.0, CAN-FD, single-channel LVDS, MIPI DSI and MIPI CSI for connecting a camera are available. An on-board Wireless Module (optional) is provided as assembly options.

The typical design power ranges from 2 W to 4 W. The module is compliant with the new SMARC 2.2 standard, allowing easy integration with SMARC baseboards. For evaluation and design-in of the SMARC-iMX93 module, Embedian provides a development platform and a starter kit. Support for Yocto Linux is available.

The module is the ideal choice for a broad range of target markets including

- Audio and Speech Recognition
- Low-cost Gateway
- Domain Controller Compute Off-load Engine
- Public Address Systems
- Audio/Video (AV) Receivers
- Soundbar
- Wireless or Networked Speakers
- And more

Complete and cost-efficient Embedian evaluation kits for Yocto build allows

immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

1.1 Features and Functionality

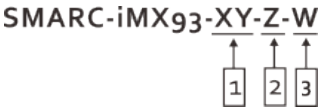
The *SMARC-iMX93* module is based on the *i.MX93* processor with dual cores Cortex-A55 from NXP. This processor offers a high number of interfaces. The module has the following features:

- *SMARC* 2.2 compliant in an 82mm x 50mm form factor.
- *NXP i.MX93* Processor:
  - *Dual x 1.7GHz ARM Cortex™-A55*
  - *Real-time 250Mhz ARM Cortex™-M33*
  - ARM Ethos™-U65 microNPU (ML) 0.5 TOPS
  - PXP 2D GPU
- Memory:
  - Onboard 16GB *eMMC* Flash
  - Onboard 16-bit 1GB or 2GB *LPDDR4*
- Networking: 2 x 10/100/1000 Mbps Ethernet (1 Gbit Ethernet QoS with TSN supports)
- Display:
  - One 24-bit Single channel *LVDS* up to 1366x768@60Hz or 1280x800@60Hz.
  - *MIPI-DSI* up to 1080p60
- Expansion: 1 x *SDHC/SDIO*, 5x *USB* 2.0 (one OTG)
- USB: 4 x *USB* 2.0 Host, 1 x *USB* 2.0 OTG
- A single 4KB *EEPROM* is provided on I2C_GP that holds the board information. This information includes board name, serial number, and revision information.
- Additional Interface:
  - 4 x UARTs
  - 2 x SPI
  - 4 x I2C
  - 2 x I2S
  - 2 x CAN-FD
  - 2 x PWM
  - 1 x 2-Lane MIPI CSI (Camera Interface)
  - 12 x GPIOs

    - WDT
- SW Support: Linux, Yocto Build
- Power Consumption (Typcal)
    - 2W
- Thermal:
    - Commercial Temperature: 0°C ~ 70°C
    - Industrial Temperature: -40° ~85°C
- Power Supply
- 3V to 5.25V
- 1.8V module IO support (SMARC 2.2 compliant)

1.2 Module Variant

The *SMARC-iMX93* module is available with various options based on processors in this family from *NXP*, *LPDDR4* memory configuration, and operating temperature ranges.



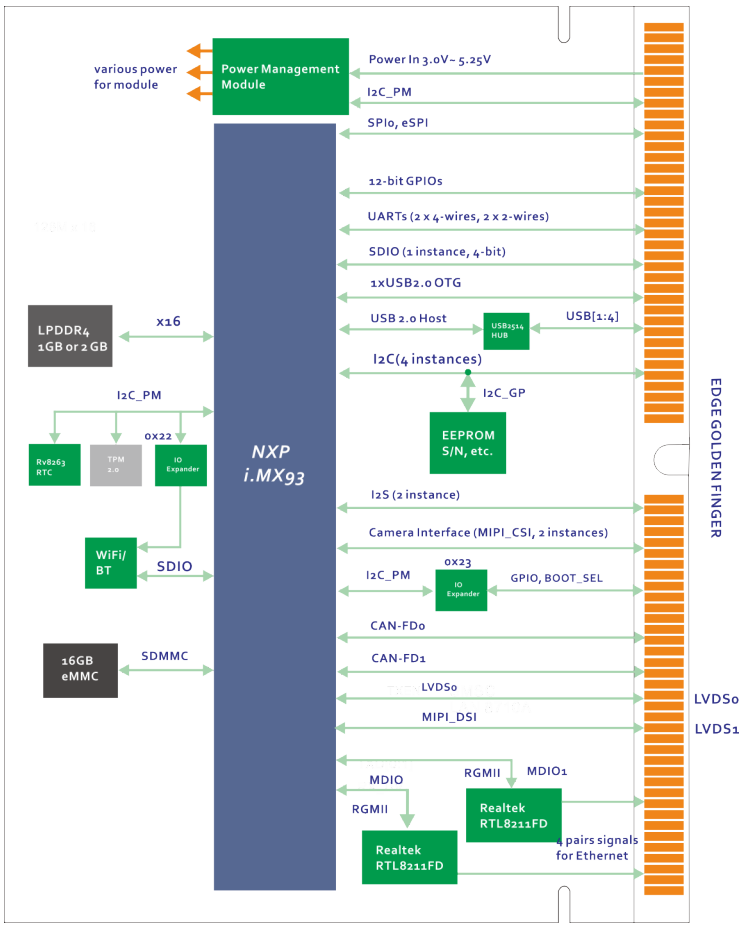
1. "*1G*" (1GB LPDDR4)
   "*2G*" (2GB LPDDR4)
2. "*I*" Industrial temperature - Leave it blank if commercial temperature.
3. "W" WiFi and Bluetooth – Leave it blank if no need.

For example, *SMARC-iMX93-1G-I* stands for 1*GB LPDDR4* memory in industrial (-40°C-85°C) operating temperature without WiFi/BT module.

1.3 Block Diagram

The following diagram illustrates the system organization of the *SMARC-iMX93*. Arrows indicate direction of control and not necessarily signal flow.

Figure 1 SMARC-iMX93 Block Diagram



Details for this diagram will be explained in the following chapters.

1.4 Software Support / Hardware Abstraction

The Embedian *SMARC-iMX93* Module is supported by Embedian BSPs (Board Support Package). BSPs for other operating systems are planned. Check with your Embedian contact or Embedian's website for the latest BSPs.

This manual goes into a lot of detail on I/O particulars – information is provided on exactly how the various *SMARC* edge fingers tie into the NXP *i.MX93* SoC and to other Module hardware. This is provided for reference and context. Almost all of the I/O particulars are covered and abstracted in the BSP and it should generally not be necessary for users to deal with I/O at the register level.

1.5 Document and Standard References

1.5.1. External Industry Standard Documents

- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (*www.jedec.org*).
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (*www.nxp.com*).
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (*www.nxp.com*).
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (*www.mxm-sig.org*).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (*www.picmg.org*).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (*www.sdcard.org*).
- ***SPI Bus –*** "Serial Peripheral Interface" - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- ***USB Specifications*** (*www.usb.org*).
- ***PCI Express Specifications (****www.pci-sig.org****)***
- ***SPDIF (aka S/PDIF) ("Sony Philips Digital Interface)****- IEC 60958-3*
- ***eSPI ("Enhanced Serial Peripheral Interface") T****he eSPI Interface Base Specification is defined by Intel (https://downloadcenter.intel.com/de/download/ 22112)*
- ***GBE MDI ("Gigabit Ethernet Medium Dependent Interface")*** *defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling defined by IEEE 802.3ab (www.ieee.org).*
- ***RS-232 (EIA "Recommended Standard 232")*** *this standard for asynchronous serial port data exchange dates from 1962. The original standard is hard to find. Many good descriptions of the standard can be found on-line, e.g. at Wikipedia, and in text books.*

- ***CSI-2 (Camera Serial Interface version 2)*** *The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Interface Alliance") (www.mipi.org).*
- ***CSI-3 (Camera Serial Interface version 3)*** *The CSI-3 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (www.mipi.org)*
- ***CAN FD ("Controller Area Network Flexible Data-Rate")*** *Bus Standard – ISO 11898-1*

1.5.2. SGET Documents

- ***SMARC_Hardware_Specification_V220,*** version 2.2, June 12, 2024
- ***SMARC_Hardware_Specification_V210,*** version 2.1, March 23, 2020
- ***SMARC_Hardware_Specification_V200***, version 2.0, June 2nd, 2016.
- ***SMARC_Hardware_Specification_V1p1***, version 1.1, May 29, 2014.
- ***SMARC_Design_Guide_V2.1.1,*** version 2.1.1, April 29, 2021

1.5.3. Embedian Documents

The following documents are listed for reference. The Module schematic is not usually available outside of Embedian, without special permission. The other schematics will be available. Contact your Embedian representative for more information. The *SMARC* Evaluation Carrier Board Schematic is particularly useful as an example of the implementation of various interfaces on a Carrier board.

- ***SMARC Evaluation Carrier Board Schematic***, PDF and OrCAD format
- ***SMARC Evaluation Carrier Board User's Manual***
- ***SMARC-iMX93 User's Manual***
- ***PinMux file for SMARC-iMX93***
- ***SMARC-iMX93 Schematic Checklist***

1.5.4. NXP Documents

- ***IMX93RM, i.MX 93 Applications Processor Reference Manual,*** *03/ 2024 (rev. 5)*
- ***IMX93IEC, i.MX 93 Industrial Applications Processor Datasheet,*** *12 / 2023 (rev. 3)*
- ***IMX93CEC, i.MX 93 Consumer Applications Processor Datasheet,*** *12 / 2023 (rev. 3)*

1.5.5. NXP Development Tools

- ***CONFIG_TOOLS_FOR_IMX v16,*** Windows Installer, rev. 16, 07/ 2024

1.5.6. NXP Software Documents

- ***Linux 6.6.23_2.0.0***

1.5.7. Embedian Software Documents

- ***Embedian Linux BSP for SMARC-iMX93 Module***
- ***Embedian Linux BSP User's Guide***
- ***Embedian Software Development Guide***

Specifications

This Chapter provides *SMARC-iMX93* specifications.

Section include：

- *SMARC-iMX93* General Functions
- *SMARC-iMX93* Debug
- Mechanical Specifications
- Electrical Specification
- Environment Specification

Chapter 2 Specifications

2.1 SMARC-iMX93 General Functions

2.1.1. SMARC-iMX93 Feature Set

This section lists the complete feature set supported by the *SMARC-iMX93* module.

SMARC Feature Specification	SMARC 2.2 Specification Maximum Number Possible	SMARC-iMX93 Feature Support	SMARC-iMX93 Feature Support Instances
LVDS LCD Display Support	2	Yes	1(single channel)
DP/eDP	1	No	N/A
HDMI Display Support	1	No	N/A
Serial Camera Support	2	Yes	2 (2 x 2-lane)
USB Interface	6	Yes	5 (1 x USB 2.0 OTG, 4 x USB 2.0)
PCIe Interface	4	No	N/A
SATA Interface	1	N/A	N/A
GbE Interface	1	Yes	1
2nd GBE Interface	1	Yes	1
SDIO Interface (4bit)	1	Yes	1
SPI Interface	2	Yes	2
I2S Interface	2	Yes	2
I2C Interface	6	Yes	4
Serial	4	Yes	4

SMARC Feature Specification	SMARC 2.2 Specification Maximum Number Possible	SMARC-iMX93 Feature Support	SMARC-iMX93 Feature Support Instances
CAN	2	Yes	2 (CAN-FD)
VDDIO	1.8V	1.8V	1.8V

2.1.2. Form Factor

The *SMARC-iMX93* module complies with the *SMARC* General Specification module size requirements in an 82mm x 50mm form factor.

2.1.3. CPU

The *SMARC-iMX93* implements *NXP's i.MX93 ARM Cortex-A55* and *ARM* Cortex-M33 processor.

NXP CPU	*i.MX93*
ARM Cortex-A55 cores	*2 x 1.7GHz Cortex-A55*
ARM Cortex-M33 cores	*1x 250Mhz Cortex-M33*
Memory Speed	*X 16 LPDDR4x-3733* *Inline ECC on the DDR bus*
L2 Cache	*64KB L2*
Graphic	*2D graphics capabilities within the PXP (pixel pipeline)*
NPU	*Arm Ethos™-U65 microNPU with 0.5 TOP/s Neural Network performs 256 8x8 MAC's per cycle* *• Keyword detect, noise reduction, beamforming* *• Speech recognition (i.e. Deep Speech 2)*

2.1.4. Onboard Storage

The *SMARC-iMX93* module supports a 16GB *eMMC* flash memory device, and a 32Kb I2C serial *EEPROM* on the Module *I2C_GP* (I2C3) bus. The device used is an On Semiconductor 24C32 equivalent. The Module serial EEPROM is intended to retain Module parameter information, including a module part number, revision number and serial number. The Module serial EEPROM data structure conforms to the PICMG® EEEP Embedded *EEPROM* Specification.). The onboard 16GB *eMMC* flash is used as boot media and operating systems. The module will always boot up from the onboard *eMMC* flash first. The firmware in *eMMC* flash will read the *BOOT_SEL* configuration from the boot selection and boot up the devices from that selected.

2.1.5. Clocks

A 24 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for CPU, BUS, and high-speed interfaces. For fractional PLLs, the 24 MHz clock from the oscillator can be directly used as the PLL reference clock.
A 32.768 KHz clock is required for the *i.MX93* CPU RTC (Real Time Clock) and external (RV-8263-C8) RTC.
A 24Mhz crystal is used on on-module *USB2514* USB hub.
The Realtek *RTL8211FD-CG* Ethernet PHY, *PCIe HCSL* clock generator is provided with a 25 MHz clock using a crystal in normal oscillation mode.

2.1.6 LVDS Interface

The *SMARC-iMX93* implements one 24-bit single channel *LVDS* output streams.

The LVDS Display Bridge (*LDB*) from the NXP® *i.MX93* processor found on the *SMARC-iMX93* offers one *LVDS* channels, with up to 1366x768@60Hz or 1280x800@60Hz.

Note:

There are one *LCDIF* controllers in *i.MX93* processor that supports one of the following instances.

- *MIPI DSI (up to 1920x1200@60Hz*, on *LVDS1* golden finger interface*)*
- *LVDS (default, up to 1366x768@60Hz* or *1280x800@60Hz*, on *lvds0* golden finger interface. *)*
- Parallel Display (no supported by SMARC)

The following figure shows the *LVDS LCD* block diagram.

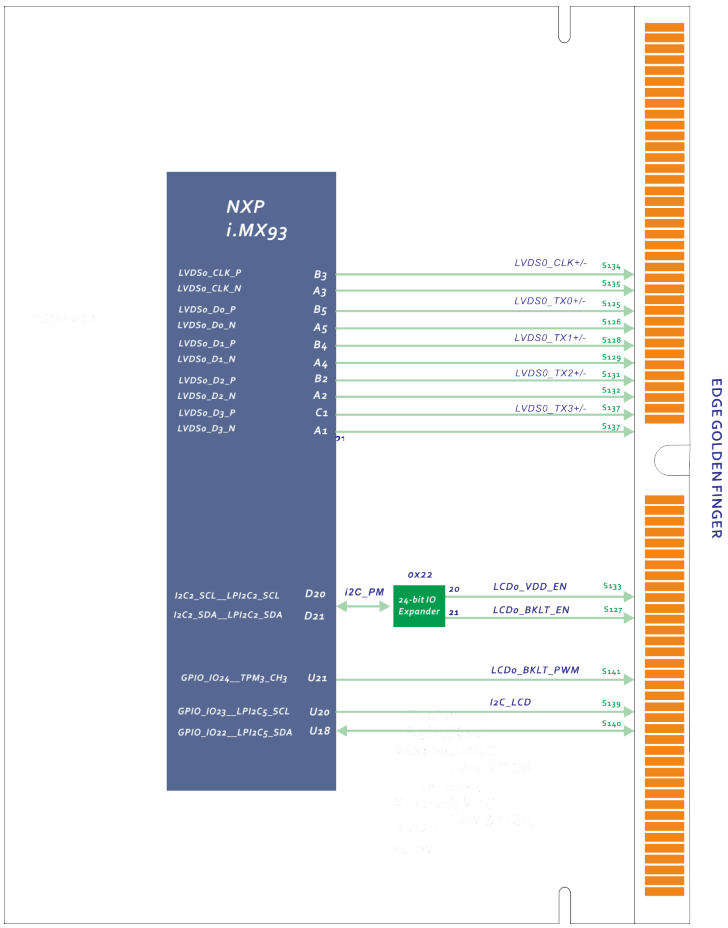


Figure 2 SMARC-iMX93 LVDS LCD Diagram

2.1.6.1 LVDS Signals

The LVDS signals data flow from i.MX93 processor to the golden finger connector is shown in the following table:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Note
Ball	Mode	Pin Name	Pin#	Net Name	
B5	N/A	LVDS_D0_P	S125	LVDS0_D0+	LVDS0 LCD data channel differential pairs 1
A5	N/A	LVDS_D0_N	S126	LVDS0_D0-	
B4	N/A	LVDS_D1_P	S128	LVDS0_D1+	LVDS0 LCD data channel differential pairs 2
A4	N/A	LVDS_D1_N	S129	LVDS0_D1-	
B2	N/A	LVDS_D2_P	S131	LVDS0_D2+	LVDS0 LCD data channel differential pairs 3
A2	N/A	LVDS_D2_N	S132	LVDS0_D2-	
C1	N/A	LVDS_D3_P	S137	LVDS0_D3+	LVDS0 LCD data channel differential pairs 4
B1	N/A	LVDS_TX3_N	S138	LVDS0_D3-	
B3	N/A	LVDS_CLK_P	S134	LVDS0_CK+	LVDS0 LCD differential clock pairs
A3	N/A	LVDS_CLK_N	S135	LVDS0_CK-	

A 24 bit single channel *LVDS* implementation comprises 5 differential pairs: 4 pairs for control data and 1 pair for the *LVDS* clock.

2.1.6.2 Other LCD Control Signals

The signals in the table below support the *LVDS LCD* interfaces.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
LCD0_VDD_EN	Output	CMOS 1.8V	High enables LVDS0 panel VDD
LCD0_BKLT_EN	Output	CMOS 1.8V	High enables LVDS0 panel backlight
LCD0_BKLT_PWM	Output	CMOS 1.8V	LVDS0 display backlight PWM control
I2C_LCD_DAT	Bi-Dir OD	CMOS 1.8V	I2C data – to read LCD display EDID EEPROMs
I2C_LCD_CK	Output	CMOS 1.8V	I2C clock – to read LCD display EDID EEPROMs

Below list *LCD* control signals that mapping to *CPU* iomux and *SMARC* edge connector.

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Port 21 of i2c GPIO Expander A			S127	LCD0_BKLT_EN	LCD0_ BKLT_EN	High enables lvds0 panel backlight
Port 20 of i2c GPIO Expander A			S133	LCD0_VDD_EN	LCD0_ VDD_EN	High enables lvds0 panel VDD
U21	ALT4	GPIO_IO24__ TPM3_CH3	S141	LCD0_BKLT_ PWM	LCD0_ BKLT_ PWM	Lvds0 display backlight PWM control
U20	ALT16	GPIO_IO23__ LPI2C5_SCL	S139	I2C_LCD_CK	I2C_ LCD_CK	I2C data – to read LCD display EDID EEPROMs
U18	ALT16	GPIO_IO22__ LPI2C5_SDA	S140	I2C_LCK_DAT	I2C_ LCD_DAT	I2C data – to read LCD display EDID EEPROMs

2.1.7 USB Interface

The *Embedian SMARC-iMX93* module supports five *USB 2.0* ports (*USB 0:4*). A Microchip *USB2514* is used to expand four *USB 2.0* ports from *i.MX93 USB2 2.0* Host Port. Per the *SMARC* specification, the module supports a USB "*On-The-Go*" (*OTG*) port capable of functioning either as a client or host device, on the *SMARC USB0* port.

The following figure shows the *USB 0:4 (USB2.0)* block diagram.

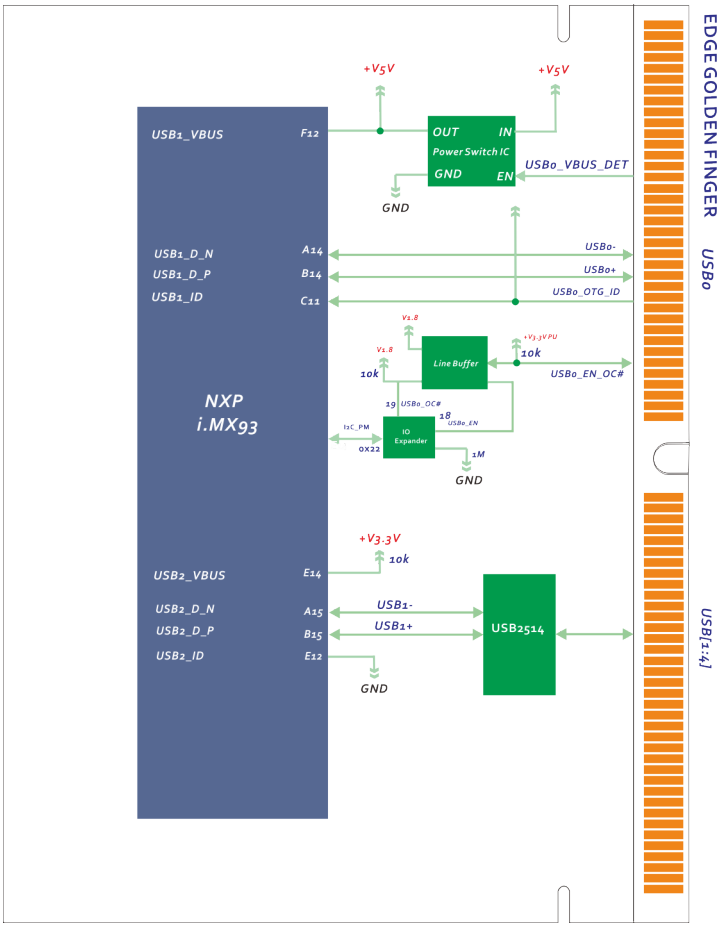


Figure 3. USB0 and USB1 Block Diagram

USB interface signals are exposed on the *SMARC-iMX93* edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
USB0 Port (USB 2.0 OTG)						
B14		USB1_D_P	P60	USB0+	USB0+	USB0 data pair
A14		USB1_D_N	P61	USB0-	USB0-	
Port 18 (USB_EN) and Port 19 (USB_OC#) of i2c IO expander A			P62	USB0_EN_OC#	USB0_EN_OC#	USB0 enable and over current pin
F12		Turn on USB_OTG_VBUS	P63	USB0_VBUS_DET	USB0_VBUS_DET	USB0 host power detection, when this port is used as a device.
C11		USB1_ID	P64	USB0_OTG_ID	USB0_OTG_ID	USB0 OTG ID input, active high

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
USB[1:4] Port (USB 2.0 Host)						
			P65	USB1+	USB1+	USB_DN3 of USB2514
			P66	USB1-	USB1-	
From USB2514			P67	USB1_EN_OC#	USB1_EN_OC#	USB1 power enable/over current indication signal
			P69	USB2+	USB2+	USB_DN1 of USB2514
			P70	USB2-	USB2-	
From USB2514			P71	USB2_EN_OC#	USB2_EN_OC#	USB2 power enable/over current indication signal
			S68	USB3+	USB3+	USB_DN2 of USB2514
			S69	USB3-	USB3-	
From USB2514			P74	USB3_EN_OC#	USB3_EN_OC#	USB3 power enable/over current indication signal
			S35	USB4+		USB_DN4 of USB2514
			S36	USB4-		
From USB2514			P76	USB4_EN_OC#	USB4_EN_OC#	USB4 power enable/over current indication signal

Note:

1. If using *USB Type-C* connector, a *PTN5110* cc logic needs to be added in your carrier board. Please refer to *i.MX93* evaluation board from NXP. The *USB Type-C* specification describes how the *USB* device uses pull-down/pull-up resistors on configuration channel pins to signify that it is a device or host.

2.1.7.1 USB Signals

The table below shows the USB related signals.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
USB[0:4]+ USB[0:4]-	Bi-Dir	USB	Differential US 2.0 Data Pair
USB[0:4]_EN_OC#	Bi-Dir OD	CMOS 3.3V	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A 10k pull-up is present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.1.7.2 USBx_EN_OC# Discussion below.
USB0_VBUS_DET USB1_VBUS_DET	Input	USB VBUS 5V	USB host power detection, when this port is used as a device.
USB0_OTG_ID	Input	CMOS 3.3V	USB OTG ID input, active high.

2.1.7.2 USB[0:3]_EN_OC# Discussion

The Module *USB[0:3]_EN_OC#* pins are multi-function Module pins, with a *10k* pull-up to a 3.3V rail on the Module, an OD driver on the Module, and, if the OC# (over-current) monitoring function is implemented on the Carrier, an *OD* driver on the Carrier. The use is as follows:

1) On the Carrier board, for external plug-in *USB* peripherals (*USB* memory sticks, cameras, keyboards, mice, etc.) *USB* power distribution is typically handled by USB power switches such as the Texas Instruments *TPS2052B* or the *Micrel MIC2026-1* or similar devices. The Carrier implementation is more straightforward if the Carrier *USB* power switches have active-high power enables and active low open drain *OC#* outputs (as the *TI* and *Micrel* devices referenced do). The USB power switch Enable and *OC#* pins for a given *USB* channel are tied together on the Carrier. The *USB* power switch enable pin must function with a low input current. The *TI* and *Micrel* devices referenced above require 1 microampere or less, at a *3.3V* enable voltage level.
2) The Module drives *USB[0:3]_EN_OC#* low to disable the power delivery to the *USBx* device.
3) The Module floats *USB[0:3]_EN_OC#* to enable power delivery. The line is pulled to *3.3V* by the Module pull-up, enabling the Carrier board *USB* power switch.
4) If there is a *USB* over-current condition, the Carrier board USB power switch drives the *USB[0:3]_EN_OC#* line low. This removes the over-current condition (by disabling the *USB* switch enable input), and allows Module software to detect the over-current condition.
5) The Module software should look for a falling edge interrupt on *USB[0:3]_EN_OC#*, while the port is enabled, to detect the *OC#* condition. The *OC#* condition will not last long, as the *USB* power switch is disabled when the switch IC detects the *OC#* condition.
6) If the *USB* power to the port is disabled (*USB[0:3]_EN_OC#* is driven low by the Module) then the Module software is aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).

Carrier Board *USB* peripherals that are not removable often do not make use of *USB* power switches with current limiting and over-current detection. It is usually

deemed un-necessary for non-removable devices. In these cases, the *USB[0:3]_EN_OC#* pins may be left unused, or they may be used as *USB[0:3]* power enables, without making use of the over-current detect Module input feature.

The *SMARC-iMX8MM* Module USB power enable and over current indication logic implementation is shown in the following block diagram. There are 10k pull-up resistors on the Module on the *SMARC USB[0:3]_EN_OC#* lines. Outputs driving the *USBx_EN_OC#* lines are open-drain. The Carrier board USB power switch, if present, is enabled by *USB[0:3]_EN_OC#* after a device connection is detected on the *DP/DM* lines.

The Enable pin on the Carrier board *USB* power switch must be active high and the Over-Current pin (*OC#*) must be open drain, active low (these are commonly available). No pull-up is required on the USB power switch Enable or *OC#* line on carrier board; they are tied together on the Carrier and fed to the Module *USB[0:3]_EN_OC#* pin.

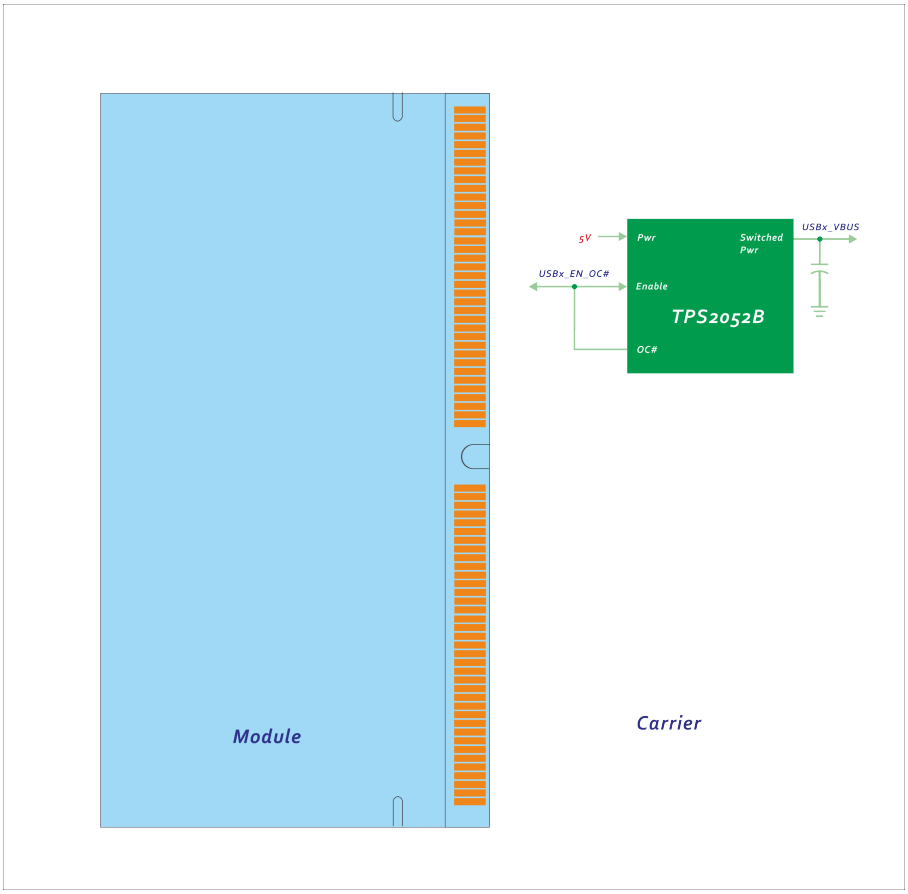


Figure 4. USB Power Distribution Implementation on Carrier

2.1.8. Gigabit Ethernet Controller (10/100/1000Mbps) Interface

The *SMARC-iMX93* module supports two Gigabit Ethernet (*10/100/1000*Mbps) interfaces, one (*GBE0*) supporting Time Sensitive Networking (*TSN*), drive gateway applications with low latency. The Gigabit Ethernet controller interfaces are accomplished by using the low-power Realtek *RTL8211FD-CG* physical layer (PHY) transceiver with variable I/O voltage that is compliant with the *IEEE 802.3-2005* standards. The *RTL8211FD-CG* supports communication with an Ethernet MAC via a standard *RGMII* interface.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from *GBE0(1)_MDIO±* to *GBE0(1)_MDI3±* plus control signals for link activity indicators. These signals can be used to connect to a *10/100/1000* BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

This is diagrammed below.

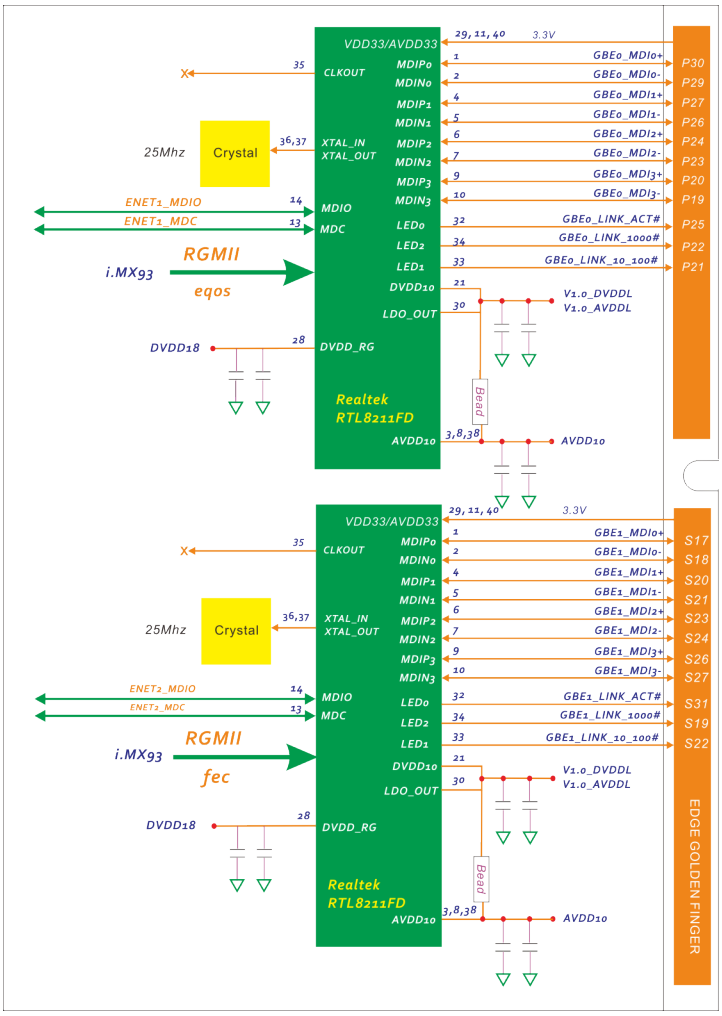


Figure 5 Gigabit Ethernet Connection from i.MX93 to Realtek RTL8211FD-CG

2.1.8.1. Path of Gigabit LAN1

i.MX93 processor and the first Realtek *RTL8211FD-CG* implementation is shown in the following table:

NXP i.MX93 CPU			Realtek RTL8211FD-CG		Net Names	Note
Ball	**Mode**	**Pin Name**	**Pin#**	**Pin Name**		
Gigabit LAN1						
AA10	ALT0	ENET1_MDIO__ ENET_QOS_MDIO	14	MDIO	ENET1_MDIO	Serial Management Interface data input/output
AA11	ALT0	ENET1_MDC__ ENET_QOS_MDC	13	MDC	ENET1_MDC	Serial Management Interface clock
AA8	ALT0	ENET1_RD0__ ENET_QOS_RGMII_RD0	25	RXD0	ENET1_RD0	Bit 0 of the 4 data bits that are sent by the transceiver on the receive path.
Y9	ALT0	ENET1_RD1__ ENET_QOS_RGMII_RD1	24	RXD1	ENET1_RD1	Bit 1 of the 4 data bits that are sent by the transceiver on the receive path.
AA9	ALT0	ENET1_RD2__ ENET_QOS_RGMII_RD2	23	RXD2	ENET1_RD2	Bit 2 of the 4 data bits that are sent by the transceiver on the receive path.
Y10	ALT0	ENET1_RD3__ ENET_QOS_RGMII_RD3	22	RXD3	ENET1_RD3	Bit 3 of the 4 data bits that are sent by the transceiver on the receive path.
AA7	ALT0	ENET1_RXC__ CCM_ENET_QOS_CLOCK _GENERATE_RX_CLK	27	RXC	ENET1_RXC	Reference clock
Y8	ALT0	ENET1_RX_CTL__ ENET_QOS_RGMII_RX_ CTL	26	RXCTL	ENET1_RX_ CTL	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the

						RGMII specification.
NXP i.MX93 CPU			**Realtek RTL8211FD-CG**		**Net Names**	**Note**
Ball	**Mode**	**Pin Name**	**Pin#**	**Pin Name**		
Gigabit LAN1						
V10	ALT0	ENET1_TX_CTL__ ENET_QOS_RGMII_TX_ CTL	19	TXCTL	ENET1_TX_ CTL	Indicates that valid transmission data is present on TXD[3:0].
W11	ALT0	ENET1_TD0__ ENET_QOS_RGMII_TD0	18	TXD0	ENET1_TD0	The MAC transmits data to the transceiver using this signal.
T12	ALT0	ENET1_TD1__ ENET_QOS_RGMII_TD1	17	TXD1	ENET1_TD1	The MAC transmits data to the transceiver using this signal.
U12	ALT0	ENET1_TD2__ ENET_QOS_RGMII_TD2	16	TXD2	ENET1_TD2	The MAC transmits data to the transceiver using this signal.
V12	ALT0	ENET1_TD3__ ENET_QOS_RGMII_TD3	15	TXD3	ENET1_TD3	The MAC transmits data to the transceiver using this signal.
U10	ALT0	ENET1_TXC__ CCM_ENET_QOS_CLOCK _GENERATE_TX_CLK	20	TXC	ENET1_TXC	Used to latch data from the MAC into the PHY. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz
port 13 of i2c IO expander A			31	INT#	ENET1_INT#	LAN1 interrupt pin

The path from *RTL8211FD-CG* to the golden finger edge connector is show in the following table.

Realtek RTL8211FD-CG		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
RTL8211FD-CG PHY1					
1	MDIP0	P30	GbE_MDI0+	GBE_MDI0+	Differential Transmit/Receive Positive Channel 0
2	MDIN0	P29	GbE_MDI0-	GBE_MDI0-	Differential Transmit/Receive Negative Channel 0
		P28	GbE_CTREF	GBE_CTREF	Center tap reference voltage
4	MDIP1	P27	GbE_MDI1+	GBE_MDI1+	Differential Transmit/Receive Positive Channel 1
5	MDIN1	P26	GbE_MDI1-	GBE_MDI1-	Differential Transmit/Receive Negative Channel 1
6	MDIP2	P24	GbE_MDI2+	GBE_MDI2+	Differential Transmit/Receive Positive Channel 2
7	MDIN2	P23	GbE_MDI2-	GBE_MDI2-	Differential Transmit/Receive Negative Channel 2
9	MDIP3	P20	GbE_MDI3+	GBE_MDI3+	Differential Transmit/Receive Positive Channel 3
10	MDIN3	P19	GbE_MDI3-	GBE_MDI3-	Differential Transmit/Receive Negative Channel 3

Realtek RTL8211FD-CG		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
RTL8211FD-CG PHY1					
32	LED0	P25	GbE_LINK_ACT#	GBE_LINK_ACT#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
33	LED1	P21	GbE_LINK100#	GBE_LINK100#	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
34	LED2	P22	GbE_LINK1000#	GBE_LINK1000#	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current

2.1.8.2. Path of Gigabit LAN2

i.MX93 processor and the second Realtek *RTL8211FD-CG* implementation is shown in the following table:

NXP i.MX93 CPU			Realtek RTL8211FD-CG		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Gigabit LAN 2						
AA6	ALT0	ENET2_MDIO__ ENET1_MDIO	14	MDIO	ENET_MDIO	Serial Management Interface data input/output
Y7	ALT0	ENET2_MDC__ ENET1_MDC	13	MDC	ENET_MDC	Serial Management Interface clock
AA4	ALT0	ENET2_RD0__ ENET1_RGMII_RD0	25	RXD0	ENET_RD0	Bit 0 of the 4 data bits that are sent by the transceiver on the receive path.
Y5	ALT0	ENET2_RD1__ ENET1_RGMII_RD1	24	RXD1	ENET_RD1	Bit 1 of the 4 data bits that are sent by the transceiver on the receive path.
AA5	ALT0	ENET2_RD2__ ENET1_RGMII_RD2	23	RXD2	ENET_RD2	Bit 2 of the 4 data bits that are sent by the transceiver on the receive path.
Y6	ALT0	ENET2_RD3__ ENET1_RGMII_RD3	22	RXD3	ENET_RD3	Bit 3 of the 4 data bits that are sent by the transceiver on the receive path.
AA3	ALT0	ENET2_RXC__ ENET1_RGMII_RXC	27	RXC	ENET_RXC	Reference clock
Y4	ALT0	ENET2_RX_CTL__ ENET1_RGMII_RX_ CTL	26	RXCTL	ENET_RX_ CTL	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.

NXP i.MX93 CPU			Realtek RTL8211FD-CG		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Gigabit LAN 2						
V6	ALT0	ENET2_TX_CTL__ ENET1_RGMII_TX_CTL	19	TXCTL	ENET_TX_CTL	Indicates that valid transmission data is present on TXD[3:0].
T8	ALT0	ENET_TD0__ ENET_QOS_RGMII_ TD0	18	TXD0	ENET_TD0	The MAC transmits data to the transceiver using this signal.
U8	ALT0	ENET_TD1__ ENET_QOS_RGMII_ TD1	17	TXD1	ENET_TD1	The MAC transmits data to the transceiver using this signal.
V8	ALT0	ENET_TD2__ ENET_QOS_RGMII_ TD2	16	TXD2	ENET_TD2	The MAC transmits data to the transceiver using this signal.
T10	ALT0	ENET_TD3__ ENET_QOS_RGMII_ TD3	15	TXD3	ENET_TD3	The MAC transmits data to the transceiver using this signal.
U6	ALT0	ENET_RGMII_TXC__ CCM_ENET_QOS_ CLOCK_GENERATE_ TX_CLK	20	TXC	ENET_TXC	Used to latch data from the MAC into the PHY. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz
port 14 of i2c IO expander A			31	INT#	ENET1_INT#	LAN2 interrupt pin

The path from the second *RTL8211FD-CG* to the golden finger edge connector is show in the following table.

Realtek RTL8211FD-CG		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
RTL8211FD-CG PHY 2					
1	MDIP0	S17	GBE1_MDI0+	GBE1_MDI0+	Differential Transmit/Receive Positive Channel 0
2	MDIN0	S18	GBE1_MDI0-	GBE1_MDI0-	Differential Transmit/Receive Negative Channel 0
		S28	GBE1_CTREF	GBE1_CTREF	Center tap reference voltage
4	MDIP1	S20	GBE1_MDI1+	GBE1_MDI1+	Differential Transmit/Receive Positive Channel 1
5	MDIN1	S21	GBE1_MDI1-	GBE1_MDI1-	Differential Transmit/Receive Negative Channel 1
6	MDIP2	S23	GBE1_MDI2+	GBE1_MDI2+	Differential Transmit/Receive Positive Channel 2
7	MDIN2	S24	GBE1_MDI2-	GBE1_MDI2-	Differential Transmit/Receive Negative Channel 2
9	MDIP3	S26	GBE1_MDI3+	GBE1_MDI3+	Differential Transmit/Receive Positive Channel 3
10	MDIN3	S27	GBE1_MDI3-	GBE1_MDI3-	Differential Transmit/Receive Negative Channel 3

Realtek RTL8211FD-CG		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
RTL8211FD-CG PHY 2					
32	LED0	S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
33	LED1	S19	GBE1_LINK100#	GBE1_LINK100#	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
34	LED2	S22	GBE1_LINK1000#	GBE1_LINK1000#	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current

2.1.8.3. Gigabit LAN Signals

The table below shows the Gigabit LAN related signals.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
GBE0(1)_MDI0+ GBE0(1)_MDI0-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)
GBE0(1)_MDI1+ GBE0(1)_MDI1-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)
GBE0(1)_MDI2+ GBE0(1)_MDI2-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)
GBE0(1)_MDI3+ GBE0(1)_MDI3-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)
GBE0(1)_100#	Output	CMOS	Link Speed Indication LED for 100Mbps
	OD	3.3V	Could be able to sink 24mA or more Carrier LED current
GBE0(1)_1000#	Output	CMOS	Link Speed Indication LED for 1000Mbps
	OD	3.3V	Could be able to sink 24mA or more Carrier LED current
GBE0(1)_LINK_ACK#	Output	CMOS	Link / Activity Indication LED
	OD	3.3V	Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
GBE0(1)_CTREF	Output	Reference Voltage	Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic (not required by the Module GBE PHY)

2.1.8.4. Suggested Magnetics

Listed below are suggested magnetics.

For normal temperature (0°C ~70°C) products.

Vendor	P/N	Package	Cores	Temp	Configuration
Halo	HFJ11-1G02E	Integrated RJ45	8	0°C~70°C	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	8	-40°C~85°C	HP Auto-MDIX
Halo	TG1G-S002NZRL	24-pin SOIC-W	8	0°C~70°C	HP Auto-MDIX

For industrial temperature (-40°C ~85°C) products.

Vendor	P/N	Package	Cores	Temp	Configuration
UDE	RB1-BA6BT9WA	Integrated RJ45	8	-40°C~85°C	HP Auto-MDIX
Halo	TG1G-E012NZRL	24-pin SOIC-W	8	-40°C~85°C	HP Auto-MDIX

2.1.9 MIPI-DSI Interface

The *SMARC-iMX93* implements one 4-lane *MIPI-DSI* output streams that are shared with *LVDS1* interface that is defined in SMARC 2.0 edge connector interface.

The *MIPI-DSI LCD* signals found on the *SMARC-i.MX93* offers one 4-lane channels, with resolutions up to 1,920 x 1,200 @60 fps at 24 bpp. They are generated from *MIPI_DSI1* signals from the *NXP® i.MX93* processor.

The following figure shows the *MIPI DSI LCD* block diagram.

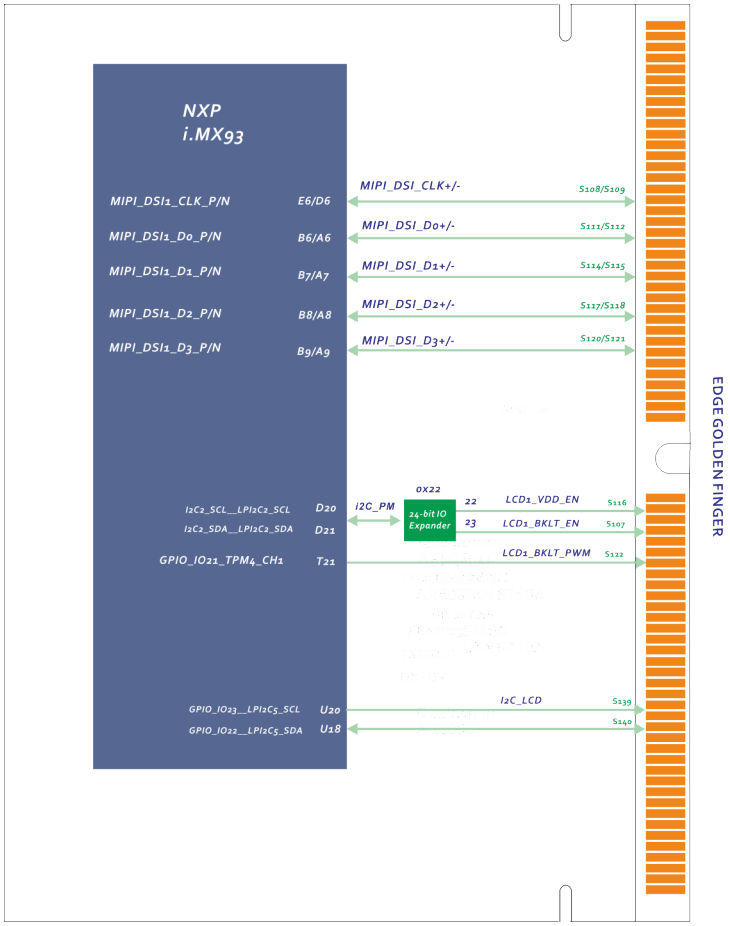


Figure 6 SMARC-iMX93 MIPI-DSI LCD Diagram

2.1.9.1 MIPI-DSI Signals Data Flow

The *MIPI-DSI* signals from *i.MX93* processor to the golden finger connector is shown in the following table:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Note
Ball	**Mode**	**Pin Name**	**Pin#**	**Net Name**	
MIPI DSI					
A16	N/A	MIPI_DSI1_D0_P	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	MIPI DSI LCD data channel differential pairs 1
B16	N/A	MIPI_DSI1_D0_N	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	
A17	N/A	MIPI_DSI1_D1_P	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	MIPI DSI LCD data channel differential pairs 2
B17	N/A	MIPI_DSI1_D1_N	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	
A19	N/A	MIPI_DSI1_D2_P	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	MIPI DSI LCD data channel differential pairs 3
B19	N/A	MIPI_DSI1_D2_N	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	
A20	N/A	MIPI_DSI1_D3_P	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	MIPI DSI LCD data channel differential pairs 4
B20	N/A	MIPI_DSI1_D3_N	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	
A18	N/A	MIPI_DSI1_CLK_P	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	MIPI DSI LCD differential clock pairs
B18	N/A	MIPI_DSI1_CLK_N	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	

2.1.9.2 MIPI DSI Signals

The table below shows the *MIPI DSI* related signals.

Edge Golden Finder Signal Name	Direction	Coupling Tolerance	Description
DSI1_LANE[0:3]+	Output	AC Coupled off module	DSI Data Pair [0:3] positive
DSI1_LANE[0:3]-	Output	AC Coupled off module	DSI Data Pair [0:3] negative

2.1.9.3 Other LCD Control Signals

The signals in the table below support the *MIPI LCD* interfaces (as these are created from the same *i.MX93* source).

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
LCD1_VDD_EN	Output	CMOS 1.8V	High enables DSI1 panel VDD
LCD1_BKLT_EN	Output	CMOS 1.8V	High enables DSI1 panel backlight
LCD1_BKLT_PWM	Output	CMOS 1.8V	DSI1 display backlight PWM control

Below list *LCD* control signals that mapping to *CPU* iomux and *SMARC* edge connector.

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Port 23 of i2c GPIO Expander A			S107	LCD1_BKLT_EN	LCD1_ BKLT_EN	High enables lvds1 panel backlight
Port 22 of i2c GPIO Expander A			S116	LCD1_VDD_EN	LCD1_ VDD_EN	High enables lvds1 panel VDD
T21	ALT6	GPIO_IO21__ TPM4_CH1	S122	LCD1_BKLT_ PWM	LCD1_ BKLT_ PWM	Lvds1 display backlight PWM control
U20	ALT16	GPIO_IO23__ LPI2C5_SCL	S139	I2C_LCD_CK	I2C_ LCD_CK	I2C data – to read LCD display EDID EEPROMs
U18	ALT16	GPIO_IO22__ LPI2C5_SDA	S140	I2C_LCK_DAT	I2C_ LCD_DAT	I2C data – to read LCD display EDID EEPROMs

2.1.10. MIPI/CMOS Serial Camera Interface (MIPI-CSI)

The *NXP® i.MX93* provides connectivity to cameras via the *MIPI/CSI-2* transmitter and maintains image manipulation and processing with adequate synchronization and control. The Camera Serial Interface (*CSI*) controls the camera port and provides interface to an image sensor or a related device. The role of the camera ports is to receive input from video sources and to provide support for time-sensitive signals to the camera. Non-time-sensitive controls such as configuration, reset are performed by the ARM platform through I2C interface or GPIO signals.

The camera interface on *SMARC-iMX93* is designed as serial interfaces on *CSI0* pin groups that can support 2 lanes providing an interface between the system and the *MIPI* D-PHY, allowing communication with an *MIPI CSI-2* compliant camera sensor.

The *MIPI-CSI2* in *SMARC-iMX93* offers a 2-lane MIPI-CSI camera interface capable of supporting 1080-p60 resolution and enables direct connection to external camera module and ISP.

The following figure shows the serial camera interface block diagram.

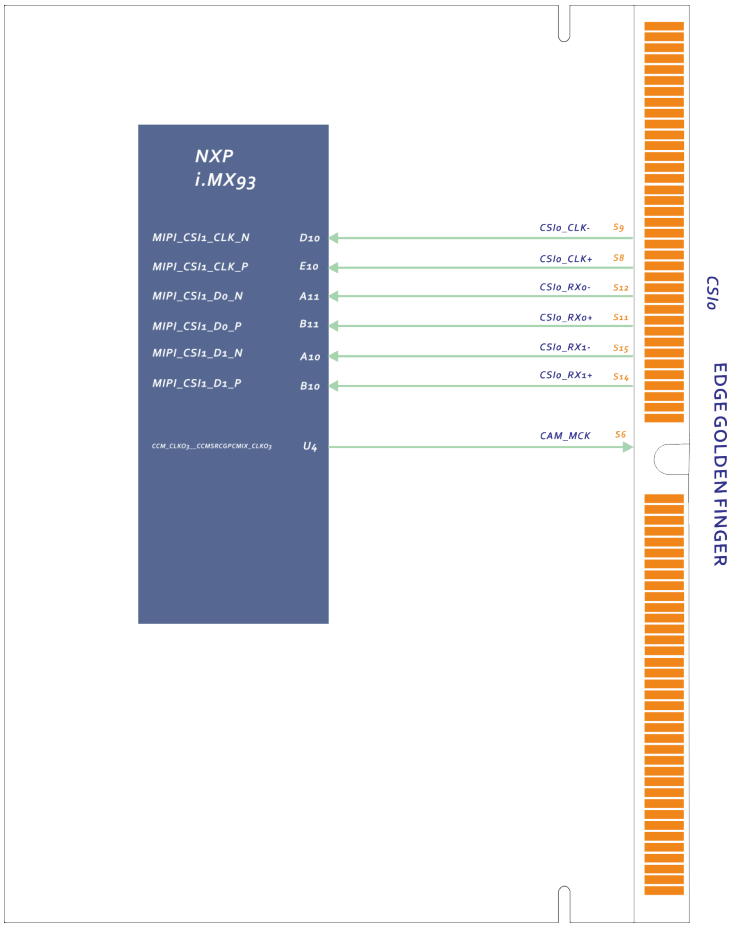


Figure 7 MIPI/Serial Camera Interface Block Diagram

MIPI/Serial Camera interface signals are exposed on the *SMARC-iMX93* edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	**Mode**	**Pin Name**	**Pin#**	**Pin Name**		
MIPI/Serial Camera Interface (CSI0)						
U4	ALT0	CCM_CLKO3__ CCMSRCGPCMIX_CLKO3	S6	CAM_MCK	CAM_MCK	Master clock output for CSI camera support
D10		MIPI_CSI1_CLK_N	S9	CSI0_CK-	CSI0_CK-	CSI0 differential clock inputs
E10		MIPI_CSI1_CLK_P	S8	CSI0_CK+	CSI0_CK+	
A11		MIPI_CSI1_D0_N	S12	CSI0_RX0-	CSI0_D0-	CSI0 differential data inputs
B11		MIPI_CSI1_D0_P	S11	CSI0_RX0+	CSI0_D0+	
A10		MIPI_CSI1_D1_N	S15	CSI0_RX1-	CSI0_D1-	
B10		MIPI_CSI1_D1_P	S14	CSI0_RX1+	CSI0_D1+	

2.1.10.1. Camera I2C Support

The I2C_CAM0 port is intended to support serial and parallel cameras. Most contemporary cameras with I2C support allow a choice of two I2C address ranges.

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
I2C_CAM0						
C20	ALT0	I2C1_SCL__ LPI2C1_SCL	S5	CSI0_TX+/ I2C_CAM0_CK	I2C_CAM0_CK	
C21	ALT0	I2C1_SDA__ LPI2C1_SDA	S7	CSI0_TX-/ I2C_CAM0_DAT	I2C_CAM0_DAT	
CSI Clock Output						
U4	ALT0	CCM_CLKO3__ CCMSRCGPCMIX_CLKO3	S6	CAM_MCK	CAM_MCK	

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
I2C_CAM0			
I2C_CAM0_DAT	Bi-Dir OD	CMOS 1.8V	Serial camera support link - I2C data
I2C_CAM0_CK	Bi-Dir OD	CMOS 1.8V	Serial camera support link - I2C clock

Note:

Embedian BSP and development board *(EVK-STD-CARRIER-S20)* supports *Coral OV5645* camera module (P/N: *G840-00180-01*, https://coral.ai/products/camera/)

2.1.10.2. MIPI Serial Camera In – MIPI CSI0

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
MIPI_CSI0_D[0:1]+ MIPI_CSI0_D[0:1]-	Input	LVDS D-PHY	CSI1 differential data inputs
MIPI_CSI0_CK+ MIPI_CSI0_CK-	Input	LVDS D-PHY	CSI1 differential clock inputs
CAM_MCK	Output	CMOS 1.8V	Master clock output for CSI1 camera support

2.1.11 SD/SDMMC Interface

SMARC-iMX93 is configured to support three *MMC* controllers. One is used for on-module 8-bit *eMMC* (*SD1*), and one is used for external *SDHC/SDIO* interface (*SD2*) and another one is used for on-module Murata *LBES5PL2EL* Wi-Fi 11a/b/g/n/ac/ax + Bluetooth 5.3 module (optional, *SD3*).

The *SMARC-iMX93* module supports one 4-bit *SDIO* interface, per the *SMARC* 2.0 specification. The *SDIO* interface uses 3.3V signaling, per the *SMARC* spec and for compatibility with commonly available *SDIO* cards.

The following figure shows the *SDIO* block diagram.

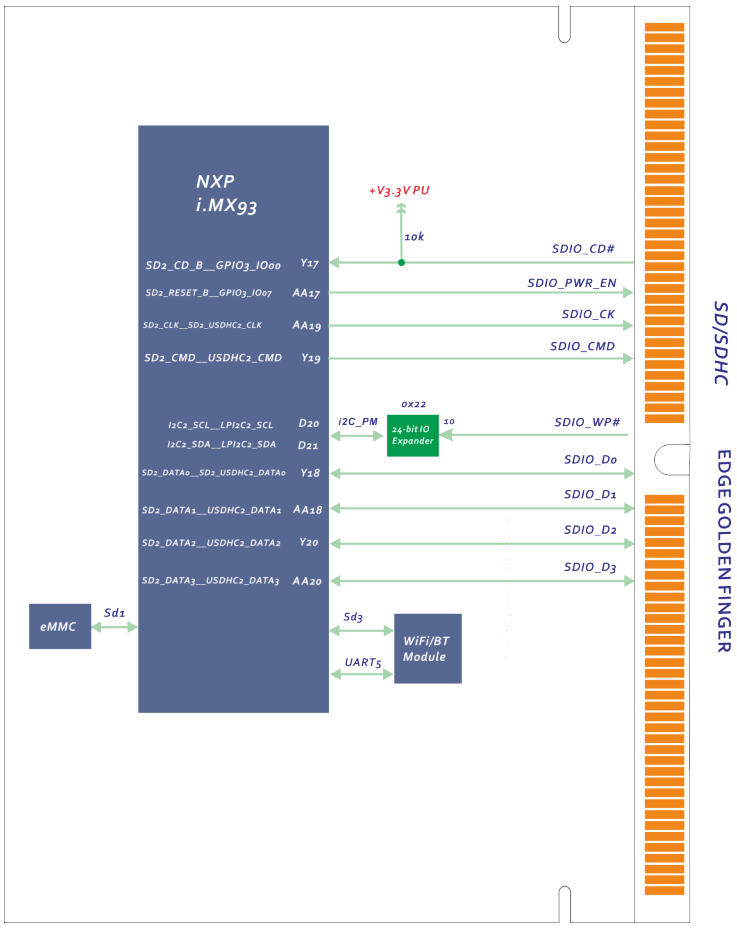


Figure 8 SD/SDIO/eMMC Interface Block Diagram

SDIO interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX8M Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SD/SDIO						
Y18	ALT0	SD2_DATA0__ USDHC2_DATA0	P39	SDIO_D0	SDIO_D0	SDIO Data 0
AA18	ALT0	SD2_DATA1__ USDHC2_DATA1	P40	SDIO_D1	SDIO_D1	SDIO Data 1
Y20	ALT0	SD2_DATA2__ USDHC2_DATA2	P41	SDIO_D2	SDIO_D2	SDIO Data 2
AA20	ALT0	SD2_DATA3__ USDHC2_DATA3	P42	SDIO_D3	SDIO_D3	SDIO Data 3
Port 10 of i2c GPIO expander A			P33	SDIO_WP	SDIO_WP	SDIO write protect signal
Y19	ALT0	SD2_CMD__ USDHC2_CMD	P34	SDIO_CMD	SDIO_CMD	SDIO Command signal
Y17	ALT5	SD2_CD_B__ GPIO3_IO00	P35	SDIO_CD#	SDIO_CD#	SDIO card detect
AA19	ALT0	SD2_CLK__ USDHC2_CLK	P36	SDIO_CK	SDIO_CK	SDIO Clock Signal
AA17	ALT5	SD2_RESET_B__ GPIO2_IO19	P37	SDIO_PWR _EN	SDIO_PWREN	SD card power enable

Note:

1. The *SDIO* card power should be switched on the Carrier board and the *SDIO* lines should be *ESD* protected. The *SMARC* Evaluation Carrier schematic is useful as an implementation reference.
2. If *SD* boot up function is required, the pull-up resistor to 3.3V of *SDIO_PWR_EN #* should be *4.7k* or less.
3. *SDIO_WP* and *SDIO_CD#* are 10k pull up to 3.3V on module.

2.1.11.1. SDIO Card (4 bit) Interface

The Carrier SDIO Card can be selected as the Boot Device (See section 4.3).

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SDIO_D[0:3]	Bi-Dir	CMOS 3.3V	4 bit data path
SDIO_CMD	Bi-Dir	CMOS 3.3V	Command Line
SDIO_CK	Output	CMOS 3.3V	Clock
SDIO_WP	Input	CMOS 3.3V	Write Protect
SDIO_CD#	Input	CMOS 3.3V	Card Detect
SDIO_PWR_EN	Output	CMOS 3.3V	SD Card Power Enable

Note:

SD Cards are not typically available with a 1.8V *I/O* voltage. The Module SD Card *I/O* level is specified as 3.3V and **not** *CMOS 1.8V*.

2.1.11.2. WiFi/BT Module (Optional)

A Murata *LBES5PL2EL* Wi-Fi 11a/b/g/n/ac/ax + Bluetooth 5.3 module is provided on *SMARC-iMX93* as an option. This section describes the path implementation.

The following figure shows the *WiFi/BT* connection block diagram.

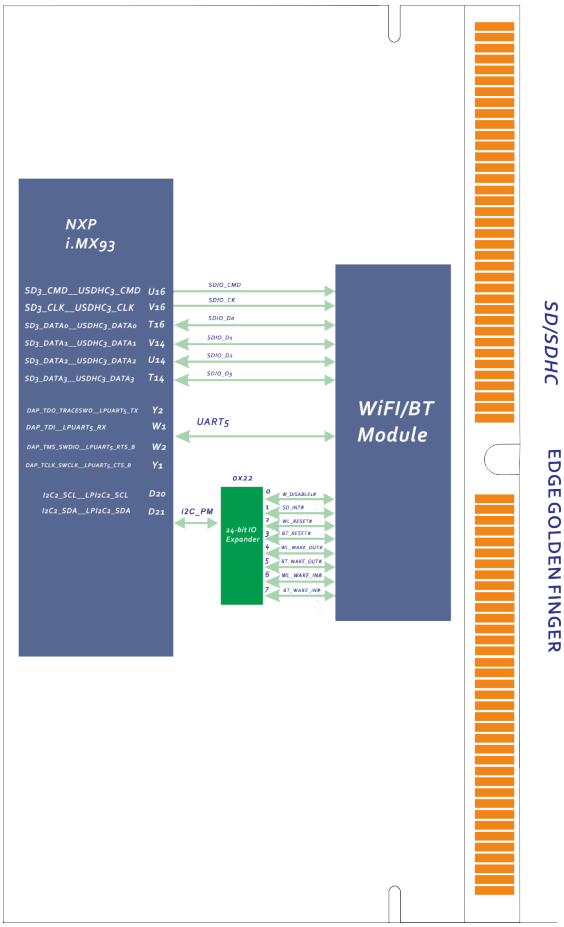


Figure 9 WiFi/BT Interface Block Diagram

i.MX93 processor and Murata *LBES5PL2EL Wi-Fi* module implementation is shown in the following table:

NXP i.MX93 CPU			Murata LBES5PL2EL		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Port 0 of i2c IO expander A Port 12 of i2c IO expander A			10	PNn	W_DISABLE1# WLAN_PWR_EN	Full Power-down (input) (active low)
U16	ALT0	SD3_CMD__ USDHC3_CMD	42	SD_CMD	SD3_CMD	SDIO Command signal
V16	ALT0	SD3_CLK__ USDHC3_CLK	44	SD_CLK	SD3_CLK	SDIO Clock signal
V14	ALT0	SD3_DATA1__ USDHC3_DATA1	45	SD_DAT[1]	SD3_DATA1	SDIO Data 1
T14	ALT0	SD3_DATA3__ USDHC3_DATA3	46	SD_DAT[3]	SD3_DATA3	SDIO Data 3
U14	ALT0	SD3_DATA2__ USDHC3_DATA2	47	SD_DAT[2]	SD3_DATA2	SDIO Data 2
T16	ALT0	SD3_DATA0__ USDHC3_DATA0	48	SD_DAT[0]	SD3_DATA0	SDIO Data 0
W1	ATL6	DAP_TDI__ LPUART5_RX	49	UART_TX	UART5_TXD	Asynchronous serial port data out
W2	ATL6	DAP_TMS_SWDIO__ LPUART5_RTS_B	50	UART_CTS	UART5_CTS#	Clear to Send handshake line
Y2	ALT6	TDO_TRACESWO__ LPUART5_TX	51	UART_RX	UART5_RXD	Asynchronous serial port data in
Y1	ALT6	DAP_TCLK_SWCLK__ LPUART5_CTS_B	52	UART_RTS	UART5_RTS#	Clear to Send handshake line

NXP i.MX93 CPU			Murata LBES5PL2EL		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Port 2 of i2c IO expander A			63	IND_RST_WL	WL_RESET#	Independent software reset for Wi-Fi
Port 3 of i2c IO expander A			64	IND_RST_BT	BT_RESET#	Independent software reset for Bluetooth
Port 1 of i2c IO expander A			72	SD_INT	SD_INT#	Out-of-band SDIO interface interrupt signal.
Port 4 of i2c IO expander			73	WL_WAKE_OUT	WL_WAKE_OUT#	Wi-Fi radio wake-up output signal.
Port 6 of i2c IO expander			74	WL_WAKE_IN	WL_WAKE_IN#	Wi-Fi radio wake-up input signal.
Port 7 of i2c IO expander			75	BT_WAKE_IN	BT_WAKE_IN#	Bluetooth/802.15.4 radio wake-up input signal.
Port 5 of i2c IO expander			76	BT_WAKE_OUT	BT_WAKE_OUT#	Bluetooth/802.15.4 radio wake-up output signal.

2.1.12 SPI/SPI1 Interface

The *SMARC-iMX93* module supports two *NXP i.MX93 SPI* interfaces (*LPSPI*) that are available off-Module for general purpose use. Each *SPI* channel has two chip-selects that can connect two SPI slave devices on each channel. *SPI* devices will share the "*SPI0_DIN*", "*SPI0_DO*" and "*SPI0_CK*" pins, but each device will have its own chip select pin. The chip select signal is a low active signal.

The *SPI* interface is diagramed below.

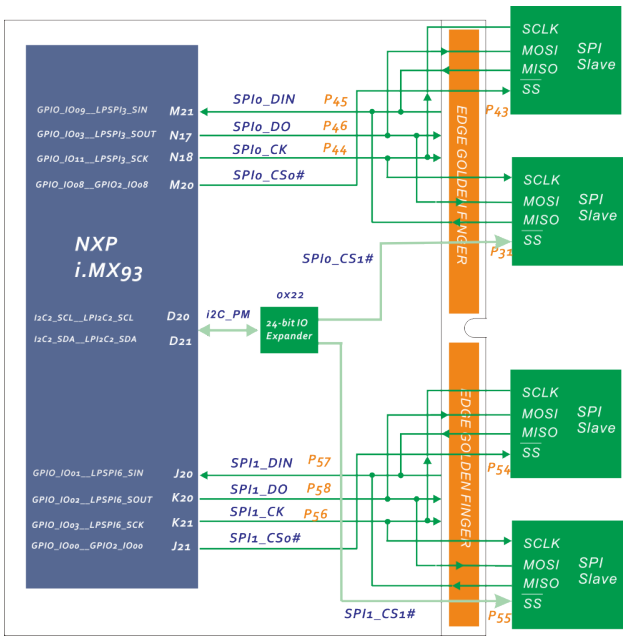


Figure 10 SPI Interface Block Diagram

SPI interface signals are exposed on the SMARC golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SPI0 Port						
M20	ALT0	GPIO_IO08__ GPIO2_IO08	P43	SPI0_CS0#	SPI0_CS0#	SPI0 Master Chip Select 0 output
Port 16 of i2c GPIO expander A			P31	SPI0_CS1#	SPI0_CS1#	SPI0 Master Chip Select 1 output
N18	ALT1	GPIO_IO11__ LPSPI3_SCK	P44	SPI0_CK	SPI0_SCLK	SPI0 Master Clock output
M21	ALT1	GPIO_IO09__ LPSPI3_SIN	P45	SPI0_DIN	SPI0_DIN	SPI0 Master Data input (input to CPU, output from SPI device)
N17	ALT1	GPIO_IO10__ LPSPI3_SOUT	P46	SPI0_DO	SPI0_DO	SPI0 Master Data output (output from CPU, input to SPI device)

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
eSPI/SPI1 Port						
J21	ALT0	GPIO_IO00__ GPIO2_IO00	P54	ESPI_CS0#	ESPI_CS0#/ SPI1_CS0#	ESPI Master Chip Select 0 output
Port 17 of i2c GPIO expander A			P55	ESPI_CS1#	ESPI_CS1#/ SPI1_CS1#	ESPI Master Chip Select 1 output
K21	ALT4	GPIO_IO03__ LPSPI6_SCK	P56	ESPI_CK	ESPI_CK/ SPI1_CK	ESPI Master Clock output
K20	ALT4	GPIO_IO02__ LPSPI6_SOUT	P58	ESPI_IO_0	ESPI_IO_0/ SPI1_DO	ESPI Master Data input (input to CPU, output from SPI device)
J20	ALT4	GPIO_IO01__ LPSPI6_SIN	P57	ESPI_IO_1	ESPI_IO_1/ SPI1_DI	ESPI Master Data output (output from CPU, input to SPI device)
			S56	ESPI_IO_2	ESPI_IO_2	Not Connected
			S57	ESPI_IO_3	ESPI_IO_3	Not Connected
			S58	ESPI_RESET#	ESPI_RESET#	Not Connected

2.1.12.1. SPI0 Signals

SMARC-iMX93 does not support *SPI0* device boot up. The Carrier *SPI0* device cannot be selected as the Boot Device – see Section 4.3 Boot Select.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SPI0_CS0#	Output	CMOS 1.8V	SPI0 Master Chip Select 0 output
SPI0_CS1#	Output	CMOS 1.8V	SPI0 Master Chip Select 1 output
SPI0_CK	Output	CMOS 1.8V	SPI0 Master Clock output
SPI0_DIN	Input	CMOS 1.8V	SPI0 Master Data input (input to CPU, output from SPI device)
SPI0_DO	Output	CMOS 1.8V	SPI0 Master Data output (output from CPU, input to SPI device)

2.1.12.2. ESPI/SPI1 Signals

SMARC-iMX93 does not support *ESPI* device boot up either. The Carrier *ESPI* device cannot be selected as the Boot Device – see Section 4.3 Boot Select.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
ESPI_CS0#/ SPI1_CS0#	Output	CMOS 1.8V	ESPI Master Chip Select 0 output
ESPI_CS1#/ SPI1_CS1#	Output	CMOS 1.8V	ESPI Master Chip Select 1 output
ESPI_CK/ SPI1_CK	Output	CMOS 1.8V	ESPI Master Clock output
ESPI_IO_[0:1]/ SPI1_[DO:DIN]	Bi-Dir	CMOS 1.8V	ESPI Master Data input/output
ESPI_RESET#	Output	CMOS 1.8V	Not Supported
ESPI_ALERT[0:1]#	Input	CMOC 1.8V	Not Supported

2.1.13. I2S Interface

The *SMARC-iMX93* module uses *I2S* format for Audio signals. These signals are derived from the Synchronous Audio Interface (*SAI*) of the *NXP® i.MX93* processor. The Serial Audio Interface (SAI) implements a synchronous serial bus interface for connecting digital audio devices. It is by far the most common mechanism used to transfer two channels of audio data between devices within a system.

SMARC-iMX93 supports two I2S instances (I2S0 and I2S2). I2S interface signals are exposed on the *SMARC-iMX93* golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
R20	ALT1	GPIO_IO17__ SAI3_MCLK	S38	AUDIO_MCK	AUD_MCLK	Master clock output to Audio codecs
I2S0 interface						
V20	ALT7	GPIO_IO26__SAI 3_TX_SYNC	S39	I2S0_LRCK	I2S0_LRCK	Left& Right audio synchronization clock
R17	ALT7	GPIO_IO19__ SAI3_TX_DATA0 0	S4 0	I2S0_SDOUT	I2S0_SDOUT	Digital audio Output
T20	ALT1	GPIO_IO20__ SAI3_RX_DATA0 0	S41	I2S0_SDIN	I2S0_SDIN	Digital audio Input
R21	ALT1	GPIO_IO16__SAI 3_TX_BCLK	S42	I2S0_CK	I2S0_CK	Digital audio clock
I2S2 interface						
G21	ALT0	SAI1_TXFS__ SAI1_TX_SYNC	S50	HDA_SYNC/ I2S2_LRCK	I2S2_LRCK	Left& Right audio synchronization clock
H21	ALT0	SAI1_TXD0__ SAI1_TX_DATA0 0	S51	HDA_SDO/ I2S2_SDOUT	I2S2_SDOUT	Digital audio Output
H20	ALT0	SAI1_RXD0__SA I1_RX_DATA00	S52	HDA_SDI/ I2S2_SDIN	I2S2_SDIN	Digital audio Input
G20	ALT0	SAI1_TXC__ SAI1_TX_BCLK	S53	HAD_CK/ I2S2_CK	I2S2_CK	Digital audio clock

Note:

SGTL5000 I2S audio codec is used in *EVK-STD-CARRIER-S20* evaluation carrier board.

2.1.13.1 I2S Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
AUDIO_MCK	Output	CMOS 1.8V	Master clock output to Audio codecs
I2S0 Signals			
I2S0_LRCK	Bi-Dir	CMOS 1.8V	Left& Right audio synchronization clock
I2S0_SDOUT	Output	CMOS 1.8V	Digital audio Output
I2S0_SDIN	Input	CMOS 1.8V	Digital audio Input
I2S0_CK	Bi-Dir	CMOS 1.8V	Digital audio clock
I2S2 Signals			
I2S2_LRCK	Bi-Dir	CMOS 1.8V	Left& Right audio synchronization clock
I2S2_SDOUT	Output	CMOS 1.8V	Digital audio Output
I2S2_SDIN	Input	CMOS 1.8V	Digital audio Input
I2S2_CK	Bi-Dir	CMOS 1.8V	Digital audio clock

2.1.14. Asynchronous Serial Port (UARTs)

The *SMARC-iMX93* module supports four UARTs (*SER0:3*). UART *SER0* and *SER2* support flow control signals (*RTS#*, *CTS#*). UART *SER1* and *SER3* do not support flow control (*TX*, *RX* only). When working with software, *SER3* is used for *SMARC-iMX93* debugging console port.

The module asynchronous serial port signals have a *VDDIO* (*1.8V*) level signal swing. If the asynchronous ports are to interface with RS232 level devices, then a Carrier RS-232 transceiver is required. The logic side of the transceiver must be able to run at 1.8V levels. The selection of 1.8V compatible transceivers is a bit limited, although more are appearing with time. Two such devices are the Texas Instruments TRS3253E, and the Maxim MAX13235E, illustrated in the figures below. The TI part is more cost effective, but has a top speed of 1 Mbps. The MAX 13235E can operate at maximum speeds over 3 Mbps. The transceivers invert the polarity of the incoming and outgoing data and handshake lines.

The other alternative is to use a level-shift IC from 1.8V to 3.3V when designing carrier board and almost all transceivers available accept a 3.3V signal level: example includes the Texas Instruments MAX3243. Note that RS232 transceivers invert the signal; a logic '1' is a negative voltage (-3.0V to -15V) and a logic '0' a positive voltage (3.0V to 15V) on the RS232 line.

Asynchronous serial ports interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	**Mode**	**Pin Name**	**Pin#**	**Pin Name**		
SER0 Port						
L17	ALT5	GPIO_IO04__ LPUART6_TX	P129	SER0_TX	SER0_TX	Asynchronous serial port data out
L18	ALT5	GPIO_IO05__ LPUART6_RX	P130	SER0_RX	SER0_RX	Asynchronous serial port data in
L20	ALT5	GPIO_IO06__ LPUART6_CTS_B	P131	SER0_RTS#	SER0_RTS#	Request to Send handshake line for SER0
L21	ALT5	GPIO_IO07__ LPUART6_RTS_B	P132	SER0_CTS#	SER0_CTS#	Clear to Send handshake line for SER0
SER1 Port						
F21	ALT0	UART2_TXD__ LPUART2_TX	P134	SER1_TX	SER1_TX	Asynchronous serial port data out
F20	ALT0	UART2_RXD__ LPUART2_RX	P135	SER1_RX	SER1_RX	Asynchronous serial port data in

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SER2 Port						
N20	ALT5	GPIO_IO12__ LPUART8_TX	P136	SER2_TX	SER2_TX	Asynchronous serial port data out
N21	ALT5	GPIO_IO13__ LPUART8_RX	P137	SER2_RX	SER2_RX	Asynchronous serial port data in
P21	ALT5	GPIO_IO15__ LPUART8_RTS_B	P138	SER2_RTS#	SER2_RTS#	Request to Send handshake line for SER2
P20	ALT5	GPIO_IO14__ LPUART8_CTS_B	P139	SER2_CTS#	SER2_CTS#	Clear to Send handshake line for SER2
SER3 Port (Debugging Port)						
E21	ALT0	UART1_TXD__ LPUART1_TX	P140	SER3_TX	SER3_TX	Asynchronous serial port data out
E20	ALT0	UART1_RXD__ LPUART1_RX	P141	SER3_RX	SER3_RX	Asynchronous serial port data in

2.1.14.1. UART Signals

Module pins for up to four asynchronous serial ports are defined. The ports are designated *SER0 – SER3*. Ports *SER0* and *SER2* are 4 wire ports (2 data lines and 2 handshake lines). Ports *SER1* and *SER3* are 2 wire ports (data only).

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SER[0:3]_TX	Output	CMOS 1.8V	Asynchronous serial port data out
SER[0:3]_RX	Input	CMOS 1.8V	Asynchronous serial port data in
SER[0]_RTS#	Output	CMOS 1.8V	Request to Send handshake line for SER0
SER[0]_CTS#	Input	CMOS 1.8V	Clear to Send handshake line for SER0
SER[2]_RTS#	Output	CMOS 1.8V	Request to Send handshake line for SER2
SER[2]_CTS#	Input	CMOS 1.8V	Clear to Send handshake line for SER2

2.1.15. I2C Interface

There is a minimum configuration of I2C ports up to a maximum of 6 ports defined in the *SMARC* specification: *PM* (Power Management), *LCD* (Liquid Crystal Display), *GP* (General Purpose), *CAM0* (Camera 0), and CAM1 (Camera 1) and *HDMI. SMARC-iMX93* supports four of these six *I2Cs* in fast mode (400 KHz operation). All *I2C* interfaces are implemented directly from *NXP i.MX93* processor interfaces.

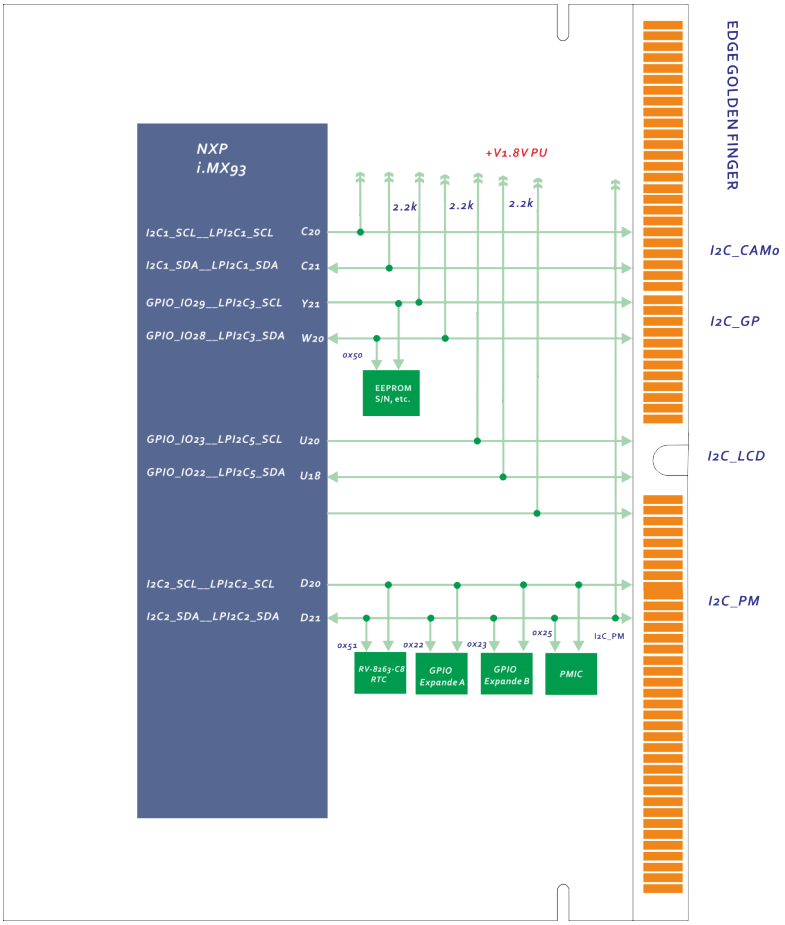


Figure 11 I2C Interface Block Diagram

This will be summarized below.

I2C Port		Primary Purpose	Alternative Use	I/O Level	Voltage
Golden Finger Connector	i.MX93 CPU				
I2C_PM	I2C2	Power Management support	System configuration management	CMOS 1.8V	
I2C_GP	I2C3	General purpose use		CMOS 1.8V	
I2C_LCD	I2C5	LCD display support, to read LCD display EDID EEPROMs (for parallel and LVDS LCD,)	General Purpose	CMOS 1.8V	
I2C_CAM0	I2C1	Serial camera 0	General Purpose	CMOS 1.8V	

Note:

The 2.2k pull-up resistors for I2C_SCL and I2C_SDA signals are on module.

The *I2C* interface signals that are exposed on the *SMARC* golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Note
Ball	**Mode**	**Pin Name**	**Pin#**	**Net Names**	
I2C_PM					
D20	ALT0	I2C2_SCL__ LPI2C2_SCL	P121	I2C_PM_CK	Power management I2C bus clock
D21	ALT0	I2C2_SDA__ LPI2C2_SDA	P122	I2C_PM_DAT	Power management I2C bus data
I2C_GP					
Y21	ALT11	GPIO_IO29__ LPI2C3_SCL	S48	I2C_GP_CK	General purpose I2C bus clock
W20	ALT11	GPIO_IO28__ LPI2C3_SDA	S49	I2C_GP_DAT	General purpose I2C bus data
I2C_LCD					
U20	ALT16	GPIO_IO23__ LPI2C5_SCL	S139	I2C_LCD_CK	LCD display I2C bus clock
U18	ATL16	GPIO_IO13__ LPI2C5_SDA	S140	I2C_LCD_DAT	LCD display I2C bus data
I2C_CAM0					
C20	ALT0	I2C1_SCL__ LPI2C1_SCL	S5	I2C_CAM0_CK	Camera 0 I2C bus clock
C21	ALT0	I2C1_SDA__ LPI2C1_SDA	S7	I2C_CAM0_DAT	Camera 0 I2C bus data

2.1.15.1. I2C GPIO Expander

There are two 24-bit I2C GPIO expanders connecting to I2C_PM bus at address *0x22* and *0x23*. Below table shows detail information.

GPIO Expander A		
Port	**Net Names**	**Description**
GPIO Expander A (0x22)		
0	W_DISABLE1#	WiFi Module Power Disable
1	SD_INT#	Out-of-band SDIO interface interrupt signal.
2	WL_RESET#	Independent software reset for Wi-Fi
3	BT_RESET#	Independent software reset for Bluetooth
4	WL_WAKE_OUT#	Wi-Fi radio wake-up output signal.
5	BT_WAKE_OUT#	Bluetooth/802.15.4 radio wake-up output signal.
6	WL_WAKE_IN#	Wi-Fi radio wake-up input signal.
7	BT_WAKE_IN#	Bluetooth/802.15.4 radio wake-up input signal.
8	TPM_IRQ#	TPM interrupt signal
9	TPM_PP	TPM physical presence
10	SD2_WP	SDIO Write Protect
11	PMIC_INT#	PMIC interrupt signal
12	WLAN_PWR_EN	WiFi module power on enable
13	ENET1_INT#	LAN1 interrupt pin

GPIO Expander A		
Port	**Net Names**	**Description**
GPIO Expander A (0x22)		
14	ENET2_INT#	LAN2 interrupt pin
15	Not used	
16	SPI0_CS1#	SPI0 Master Chip Select 1 output.
17	ESPI_CS1#	ESPI Master Chip Select 1 output.
18	USB0_EN	USB0 Power enable Pin
19	USB0_OC#	USB0 Over-Current Pin
20	LCD0_VDD_EN	LVDS VDD Power Enable Pin
21	LCD0_BKLT_EN	LVDS Backlight Enable Pin
22	LCD1_VDD_EN	MIPI-DSI VDD Power Enable Pin
23	LCD1_BKLT_EN	MIPI-DSI Backlight Enable Pin

GPIO Expander B		
Port	**Net Names**	**Description**
GPIO Expander B (0x23)		
0	GPIO0	GPIO0 pin on SMARC Golden Finger Connector (P108)
1	GPIO1	GPIO1 pin on SMARC Golden Finger Connector (P109)
2	GPIO2	GPIO2 pin on SMARC Golden Finger Connector (P110)
3	GPIO3	GPIO3 pin on SMARC Golden Finger Connector (P111)
4	GPIO4	GPIO4 pin on SMARC Golden Finger Connector (P112)
5	GPIO6	GPIO6 pin on SMARC Golden Finger Connector (P114)
6	GPIO7	GPIO7 pin on SMARC Golden Finger Connector (P115)
7	GPIO8	GPIO8 pin on SMARC Golden Finger Connector (P116)
8	GPIO9	GPIO9 pin on SMARC Golden Finger Connector (P117)
9	GPIO10	GPIO10 pin on SMARC Golden Finger Connector (P118)
10	GPIO11	GPIO11 pin on SMARC Golden Finger Connector (P119)
11	GPIO12	GPIO12 pin on SMARC Golden Finger Connector (S142)
12	GPIO13	GPIO13 pin on SMARC Golden Finger Connector (S123)
13	USB0_ID_INT#	USD0 ID Pin

GPIO Expander B		
Port	**Net Names**	**Description**
GPIO Expander B (0x23)		
14	Not used	
15	IMX_RESET_OUT	SMARC RESET_OUT#
16	LID#	Lid open/close indication to Module. (S148)
17	SLEEP#	Sleep indicator from Carrier board.(S149)
18	CHARGING#	Held low by Carrier if DC input for battery charger is present. (S151)
19	BATLOW#	Battery low indication to Module.(S156)
20	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present.(S152)
21	BOOT_SEL0#	SYSBOOT (P123)
22	BOOT_SEL1#	SYSBOOT (P124)
23	BOOT_SEL2#	SYSBOOT (P125)

Note:

All *I2C* bus defined in SMARC 2.0 specification are operated at 1.8V. The slave devices and their address details are listed in the following table:

#	Device	Description	Address (7-bit)	Address (8-bit)		Notes
				Read	Write	
I2C_GP						
1	On Semiconductor CAT24C32	EEPROM	0x50	0xA1	0xA0	General purpose parameter EEPROM, Serial number, etc in PICMG EEEP format
I2C_PM						
1	NXP PCA9451AHN	PMIC	0x25	0x4B	0x4A	Power Management IC
2.	Micro Crystal RV-8263-C8	RTC	0x51	0xA3	0xA2	Real-Time Clock
3	NXP PCAL6524HE	IO Expander A	0x22	0x45	0x44	TPM 2.0
4	NXP PCAL6524HE	IO Expander B	0x23	0x8B	0x8A	I2C IO Expander

Note:

On-module *EEPROM* has been moved from *I2C_PM* to *I2C_GP* at *SMARC 2.0 specification*.

2.1.16. CAN Bus Interface

The *FlexCAN* module in *i.MX93* processor is a communication controller implementing the CAN protocol according to the *ISO 11898-1* standard and CAN 2.0 B protocol specifications (*CAN-FD*). The Flexible Controller Area Network (*FlexCAN*) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. The *SMARC-iMX93* module supports two *CAN-FD* bus interfaces.

CAN-FD interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Note
Ball	Mode	Pin Name	Pin#	Net Names	
CAN0 BUS					
G17	ALT6	PDM_CLK__ CAN1_TX	P143	CAN0_TX	CAN0 Transmit output
J17	ALT6	PDM_BIT_STREAM0__ CAN1_RX	P144	CAN0_RX	CAN0 Receive input
CAN1 BUS					
V21	ALT2	GPIO_IO25__ CAN2_TX	P145	CAN1_TX	CAN1 Transmit output
W21	ALT2	GPIO_IO27__ CAN2_RX	P146	CAN1_RX	CAN1 Receive input

A CAN transceiver on carrier is necessary to adapt the signals from *SMARC* golden finger edge connector, which is TTL levels, to the physical layer used. Because the CAN bus system is typically used to connect multiple systems and is often run over very long distances, both power supply and signal path must be electrically isolated to meet a certain isolation level. Users can refer the "***SMARC Carrier Board Hardware Design Guide***" or CAN transceiver application note such

as TI SLLA270 for more details.

2.1.16.1. CAN0 BUS Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
CAN0_TX	Output	CMOS 1.8V	CAN0 Transmit output
CAN0_RX	Input	CMOS 1.8V	CAN0 Receive input

2.1.16.2. CAN1 BUS Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
CAN1_TX	Output	CMOS 1.8V	CAN1 Transmit output
CAN1_RX	Input	CMOS 1.8V	CAN1 Receive input

2.1.17. GPIOs

The *SMARC-iMX93* module supports *12* GPIOs, as defined by the *SMARC* specification. Specific alternate functions are assigned to some *GPIO*s such as *PWM / Tachometer* capability, Camera support, and HD Audio reset. All pins are capable of bi-directional operation. A default direction of operation is assigned, with half of them (*GPIO0 – GPIO5*) for use as outputs and the remainder (*GPIO6 – GPIO11*) as inputs by *SMARC* hardware specification.

GPIO signals are exposed on the *SMARC* golden finger edge connector as shown below:

NXP i.MX93 CPU			SMARC-iMX93 Edge Golden Finger		Net Names	Note
Ball	**Mode**	**Pin Name**	**Pin#**	**Pin Name**		
GPIOs						
Port 0 of i2c GPIO expander B			P108	GPIO0/CAM0_PWR#	GPIO0	Camera 0 Power Enable, active low output
Port 1 of i2c GPIO expander B			P109	GPIO1/CAM1_PWR#	GPIO1	Camera 1 Power Enable, active low output
Port 2 of i2c GPIO expander B			P110	GPIO2 /CAM0_RST#	GPIO2	Camera 0 Reset, active low output
Port 3 of i2c GPIO expander B			P111	GPIO3/CAM1_RST#	GPIO3	Camera 1 Reset, active low output
Port 4 of i2c GPIO expander B			P112	GPIO4/HDA_RST#	GPIO4	HD Audio Reset, active low output
G18	ALT5 ALT3	PDM_BIT_STREAM1__ GPIO01_IO10/ TPM2_EXTCLK	P113	GPIO5/PWM_OUT	GPIO5	PWM output
Port 5 of i2c GPIO expander B			P114	GPIO6/TACHIN	GPIO6	Tachometer input (used with the GPIO5 PWM)
Port 6 of i2c GPIO expander B			P115	GPIO7	GPIO7	
Port 7 of i2c GPIO expander B			P116	GPIO8	GPIO8	
Port 8 of i2c GPIO expander B			P117	GPIO9	GPIO9	
Port 9 of i2c GPIO expander B			P118	GPIO10	GPIO10	
Port 10 of i2c GPIO expander B			P118	GPIO11	GPIO11	

2.1.17.1. GPIO Signals

Twelve Module pins are allocated for *GPIO* (general purpose input / output) use. All pins are capable of bi-directional operation. By *SMARC* specification, *GPIO0 – GPIO5* are recommended for use as outputs and the remainder (*GPIO6 – GPIO11*) as inputs.
At Module power-up, the state of the GPIO pins may not be defined, and may briefly be configured in the "wrong" state, before boot loader code corrects them. Carrier designers should be aware of this and plan accordingly. All GPIO pins are capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the *i.MX93* register set.

Edge Golden Finder Signal Name	Preferred Direction	Type Tolerance	Description
GPIO0/CAM0_PWR#	Output	CMOS 1.8V	Camera 0 Power Enable, active low output
GPIO1/CAM1_PWR#	Output	CMOS 1.8V	Camera 1 Power Enable, active low output
GPIO2 /CAM0_RST#	Output	CMOS 1.8V	Camera 0 Reset, active low output
GPIO3/CAM1_RST#	Output	CMOS 1.8V	Camera 1 Reset, active low output
GPIO4/HDA_RST#	Output	CMOS 1.8V	HD Audio Reset, active low output
GPIO5/PWM_OUT	Output	CMOS 1.8V	PWM output
GPIO6/TACHIN	Input	CMOS 1.8V	Tachometer input (used with the GPIO5 PWM)
GPIO7/PCAM_FLD	Input	CMOS 1.8V	
GPIO8/CAN0_ERR#	Input	CMOS 1.8V	
GPIO9/CAN1_ERR#	Input	CMOS 1.8V	
GPIO10	Input	CMOS 1.8V	
GPIO11	Input	CMOS 1.8V	

2.1.18 Watchdog Timer Interface

i.MX93 features an internal *WDT*. Embedian's Linux kernel enables the internal *i.MX93 WDT* and makes this functionality available to users through the standard Linux Watchdog API.
A description of the API is available following the link below:
http://www.kernel.org/doc/Documentation/watchdog/watchdog-api.txt

WDT signals are exposed on the *SMARC* golden finger edge connector as shown below:

NXP i.MX93 CPU			*SMARC-iMX93 Edge Golden Finger*		*Net Names*	*Note*
Ball	*Mode*	*Pin Name*	*Pin#*	*Pin Name*		
Watchdog Timer						
Y3	*ALT5*	*CCM_CLKO2__ GPIO3_IO27*	*S145*	*WDT_TIME_ OUT#*	*WDT_TIME_OUT #*	*Watchdog-Timer Output*

2.1.19 Boot ID EEPROM

The *SMARC-iMX93* module includes an I2C serial *EEPROM* available on the *I2C_GP* bus. An On Semiconductor *24C32* or equivalent *EEPROM* is used in the module. The device operates at 1.8V. The Module serial *EEPROM* is placed at I2C slave addresses *A2 A1 A0* set to 0 (I2C slave address 50 hex, 7 bit address format or *A0 / A1* hex, 8 bit format) (for I2C *EEPROM*s, address bits *A6 A5 A4 A3* are set to binary 0101 convention).

The module serial *EEPROM* is intended to retain module parameter information, including serial number. The module serial *EEPROM* data structure conforms to the *PICMG® EEEP* Embedded *EEPROM* Specification.

Note:
The *EEPROM ID* memory layout is now follow the mainline and as follows.

Name	Size (Bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for Board in ASCII "SMC93D1G" = Dual Core Cortex-A55 and 1GB LPDDR4 Configuration operating at Commercial Temp. "SMC93I1G" = Dual Core Cortex-A55 and 1GB LPDDR4 Configuration operating at Industrial Temp. "SMC93D2G" = Dual Core Cortex-A55 and 2GB LPDDR4 Configuration operating at Commercial Temp. "SMC93I2G" = Dual Core Cortex-A55 and 2GB LPDDR4 Configuration in Industrial Temp. "SMC93D1W" = Dual Core Cortex-A55 and 1GB LPDDR4 Configuration operating at Commercial Temp. with WiFi/BT "SMC93D2W" = Dual Core Cortex-A55 and 2GB LPDDR4 Configuration operating at Commercial Temp.with WiFi/BT "SMC93I1W" = Dual Core Cortex-A55 and 1GB LPDDR4 Configuration operating at Industrial Temp.with WiFi/BT "SMC93I2W" = Dual Core Cortex-A55 and 2GB LPDDR4 Configuration operating at Industrial Temp.with WiFi/BT
Version	4	Hardware version code for version in ASCII "00A0" = rev. A0
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYY3010nnnn Where: WW = 2 digit week of the year of production YY = 2 digit year of production 3 = Module iMX93 010/01W/I10/I1W= Commercial 1G/Commercial 1G with WiFi/Industrial 1G/Industrial 1G with WiFi or 020//02W/I20/I2W= Commercial 2G/Commercial 2G with WiFi/Industrial 2G/Industrial 2G with WiFi nnnn = incrementing board number

Name	Size (Bytes)	Contents
Configuration Option	32	Codes to show the configuration setup on this board. These 32 bytes are reserved by default.
MAC Address	6	Ethernet MAC Address (10:0D:32:XX:XX:XX)
MAC Address	6	Ethernet MAC Address for 2nd LAN (10:0D:32:XX:XX:XX)
Available	32720	Available space for other non-volatile codes/data

2.2 SMARC-iMX93 Debug

2.2.1. Serial Port Debug

SMARC module has 4 serial output ports, *SER0*, *SER1*, *SER2 and SER3*. Out of these 4 serial ports, *SER3* is set as the serial debug port use for *i.MX93* from Embedian. Users can change to any port they want to from *u-boot defconfig* file. *SER3* is exposed (along with all other serial ports available on the module) in the *SMARC-iMX93* Evaluation Carrier. The default baud rate setting is *115,200 8N1*. *SER3* pin out of the *SMARC-iMX93* is shown below:

NXP i.MX93 CPU		SMARC-iMX93 Edge Golden Finger		Net Names	Notes
mode	Pin Name	Pin#	Pin Name		
SER3 (Debugging Port)					
ALT0	UART1_TXD__ LPUART1_TX	P140	SER3_TX	SER3_TX	Asynchronous serial port data out
ALT0	UART1_RXD__ LPUART1_RX	P141	SER3_RX	SER3_RX	Asynchronous serial port data in

2.3 Mechanical Specifications

2.3.1. Module Dimensions

The *SMARC-iMX93* complies with *SMARC* Hardware Specification in an 82mm x 50 mm form factor.

2.3.2. Height on Top

1.3mm maximum (without PCB) complied with *SMARC* specification defines as 3mm as the maximum.

2.3.3. Height on Bottom

0.9mm maximum (without PCB) complied with *SMARC* specification defines as 1.3mm as the maximum.

2.3.4. Mechanical Drawings

The mechanical information is shown in Figure 12: *SMARC-iMX93* Mechanical Drawings (Top View) and Figure 13: *SMARC-iMX93* Mechanical Drawings (Bottom View))

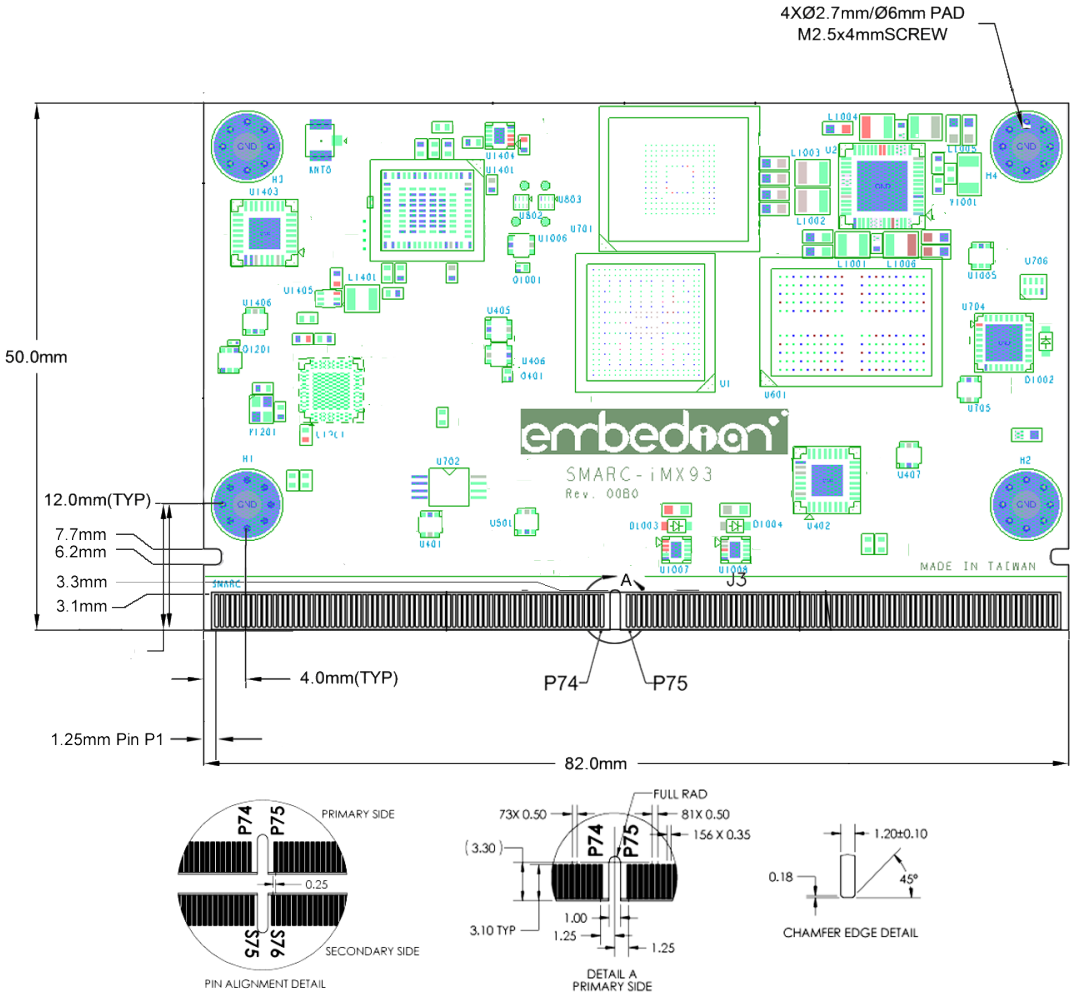


Figure 12 SMARC-iMX93 Mechanical Drawings (Top View)

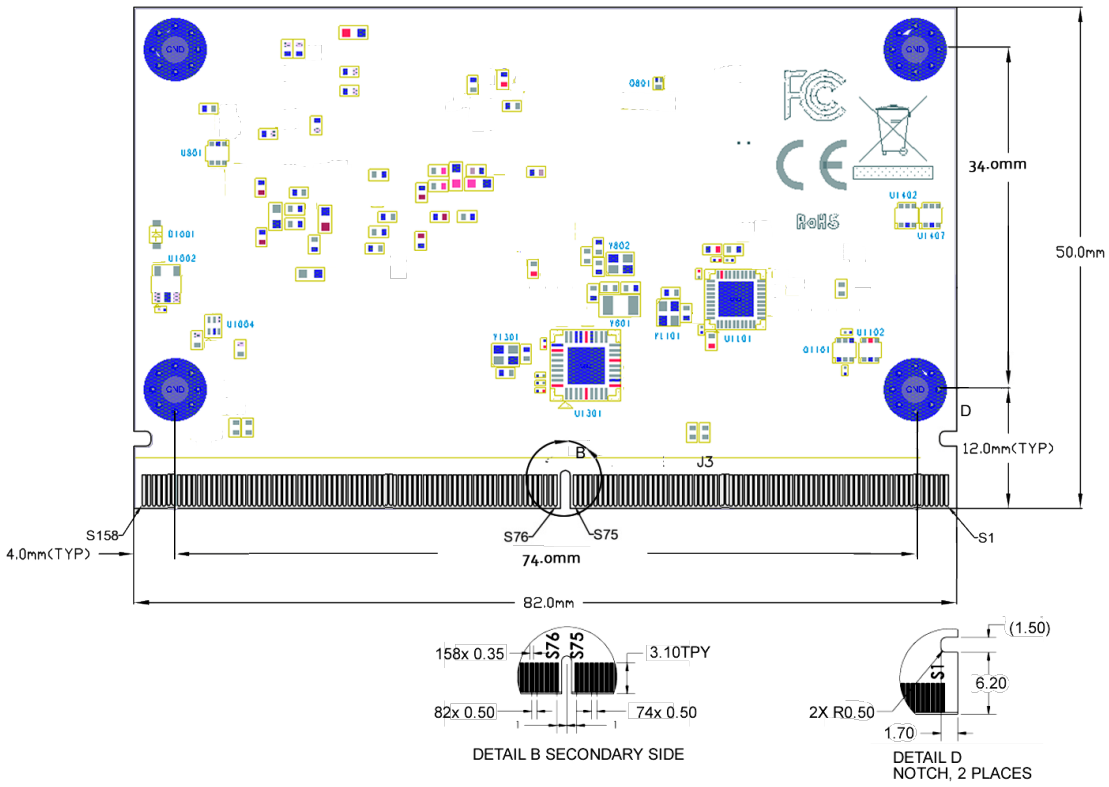


Figure 13 SMARC-iMX93 Mechanical Drawings (Bottom View)

The figure on the following page details the 82mm x 50mm Module mechanical attributes, including the pin numbering and edge finger pattern.

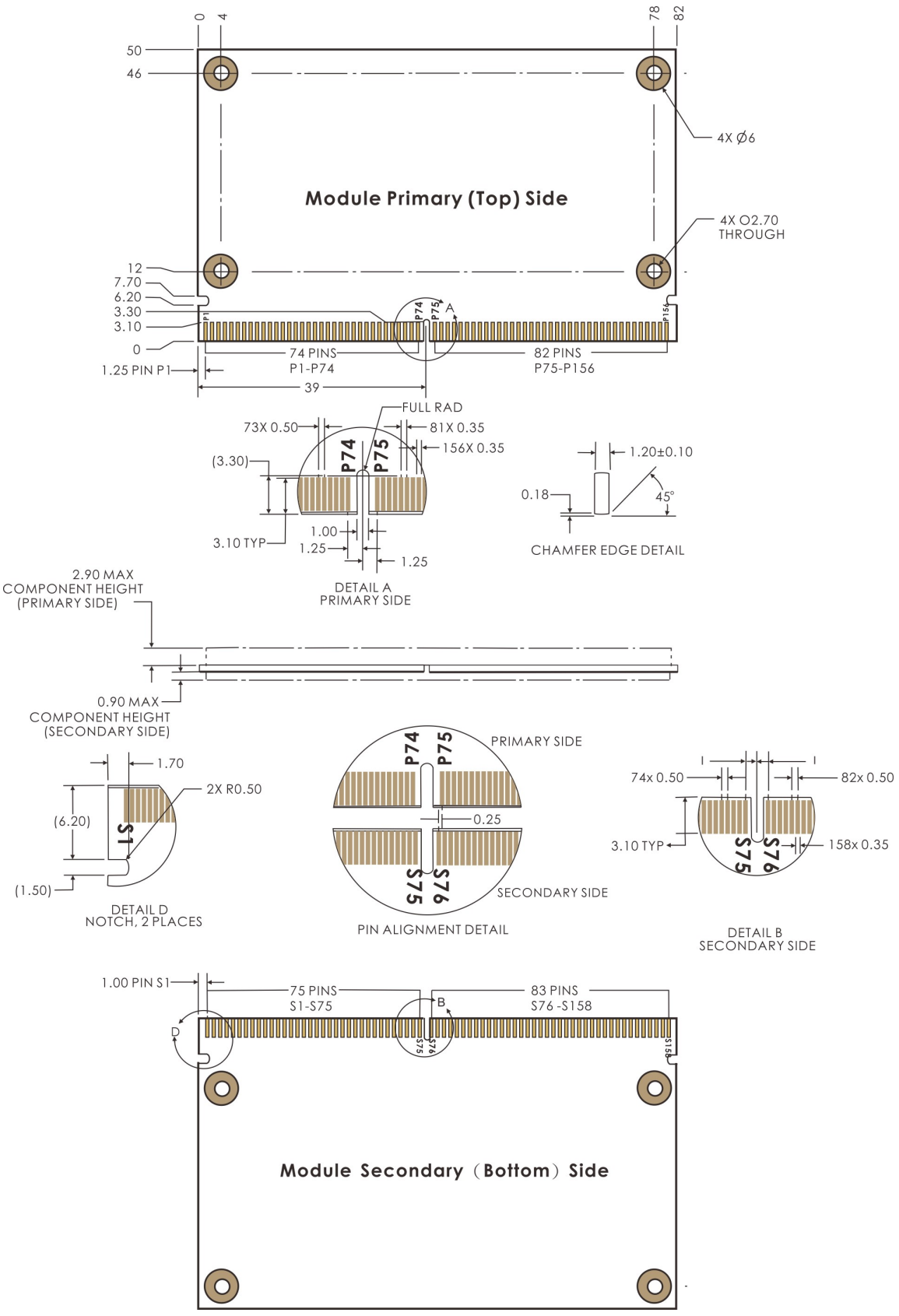


Figure 14 SMARC-iMX93 Module Mechanical Outline

Top side major component (IC and Connector) information is shown in Figure 15: *SMARC-iMX93* Top side components.

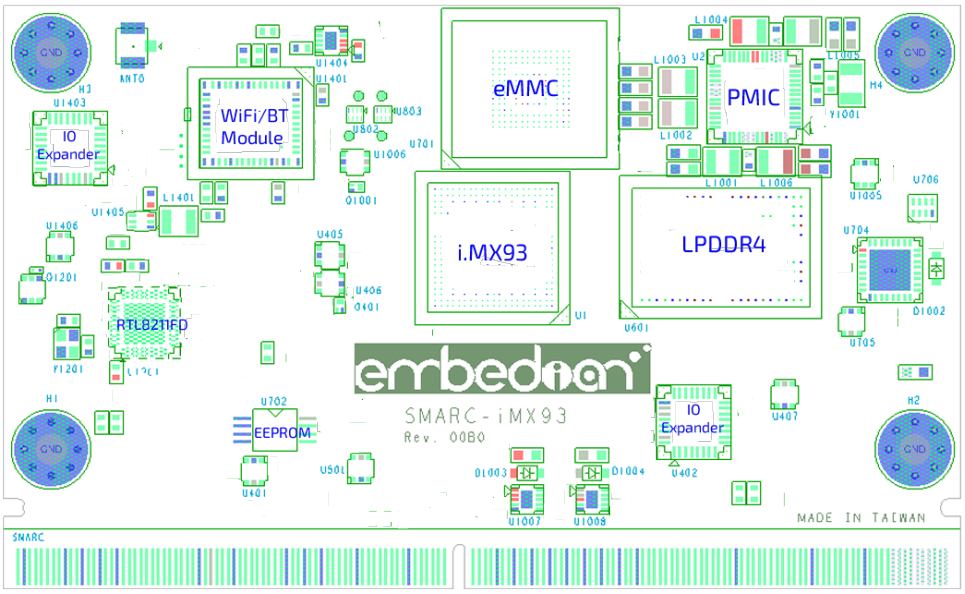


Figure 15 SMARC-iMX93 Top Side Components

Bottom side major component (IC and Connector) information is shown in Figure 16: *SMARC-iMX93* Bottom side components.

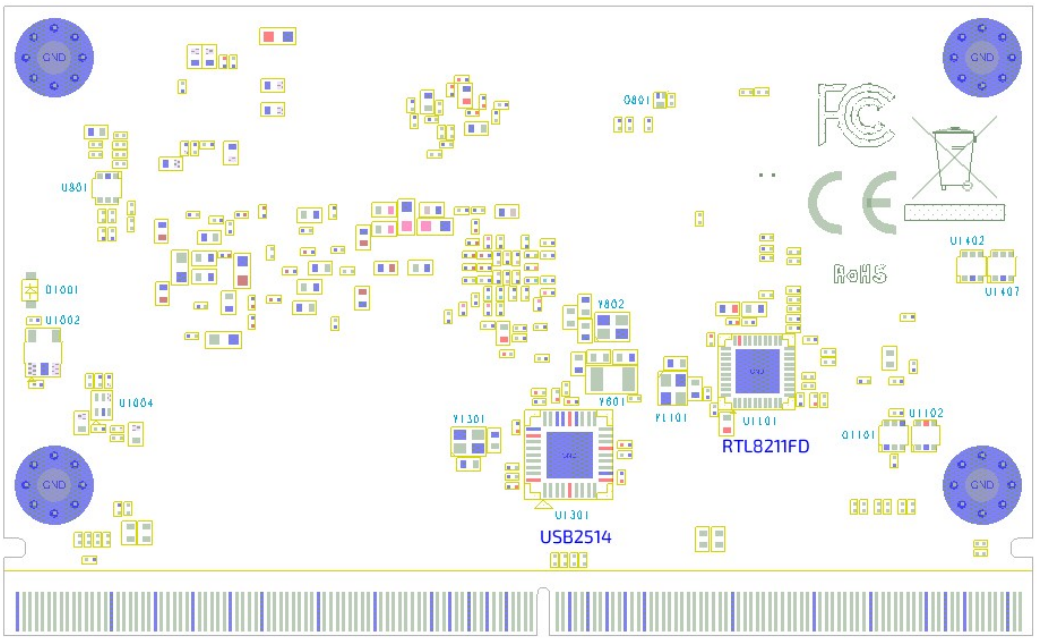


Figure 16 SMARC-iMX93 Bottom Side Components

SMARC-iMX93 height information from Carrier board Top side to tallest Module component is shown in Figure 17: *SMARC-iMX93* Minimum "Z" Height:

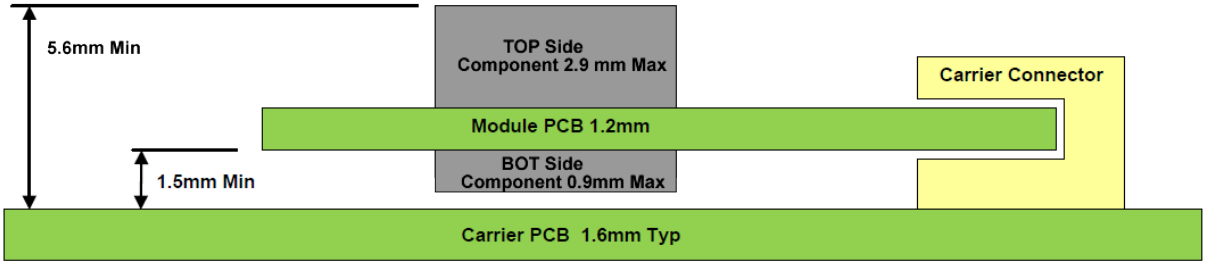


Figure 17 SMARC-iMX93 Minimum "Z" Height

The *SMARC* connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.

When a 1.5mm stack height Carrier board connector is used, there shall not be components on the Carrier board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there should not be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that may protrude through the Module.

If Carrier board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module-to-Carrier connector may be used. Stack heights of 2.7mm, 3mm, 5mm and up are available.

2.3.5. Carrier Board Connector PCB Footprint

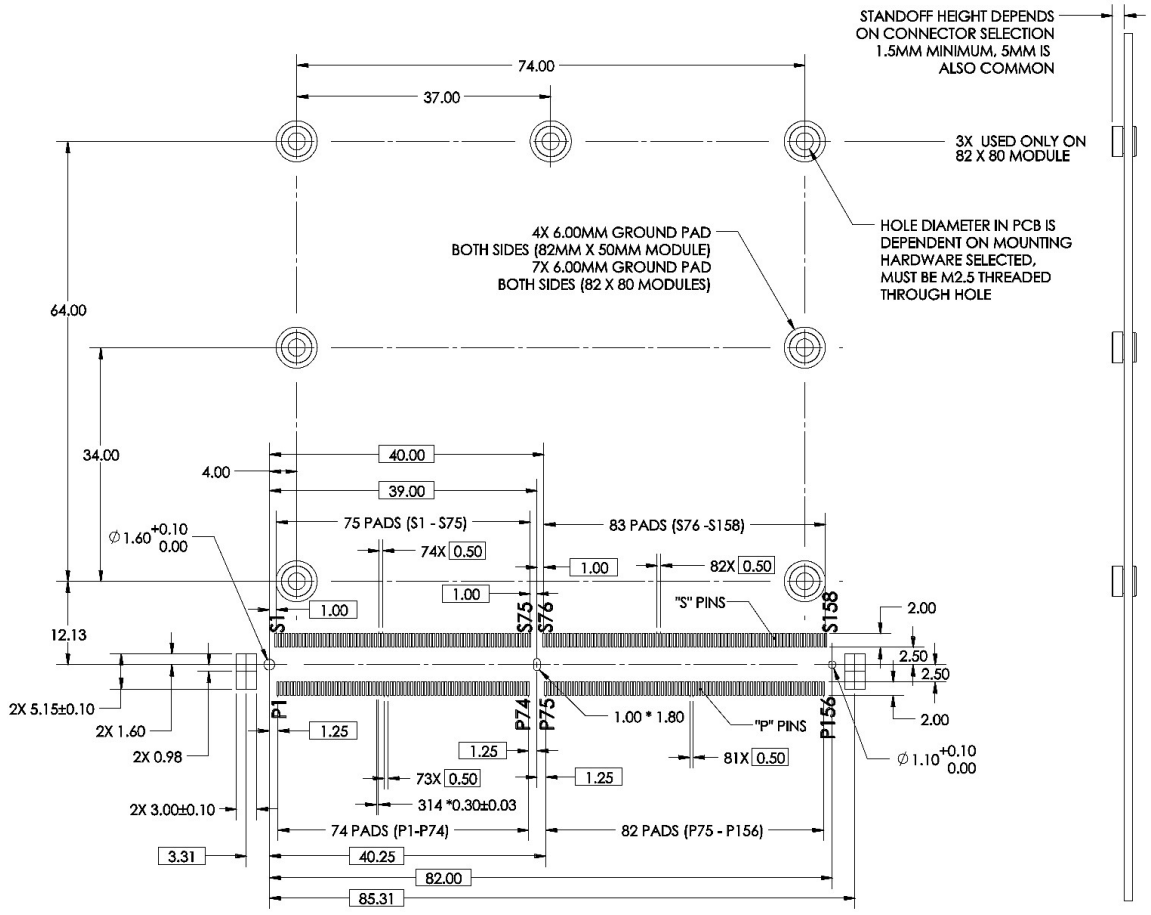


Figure 18 Carrier Board Connector PCB Footprint

Note:

The hole diameter for the 4 holes (82mm x 50mm Module) or 7 holes (82mm x 80mm Module) depends on the spacer hardware selection. See the section below for more information on this.

2.3.6. Module Assembly Hardware

The *SMARC-iMX93* module is attached to the carrier with four M2.5 screws. A 4mm length screw is usually used. The attachment holes are located on the corners of the module. Attachment holes have a 6mm diameter pad, 2.7 mm dia drill hole as shown Figure 12: *SMARC-iMX93* Mechanical Drawings (Top View)

2.3.7. Carrier Board Standoffs

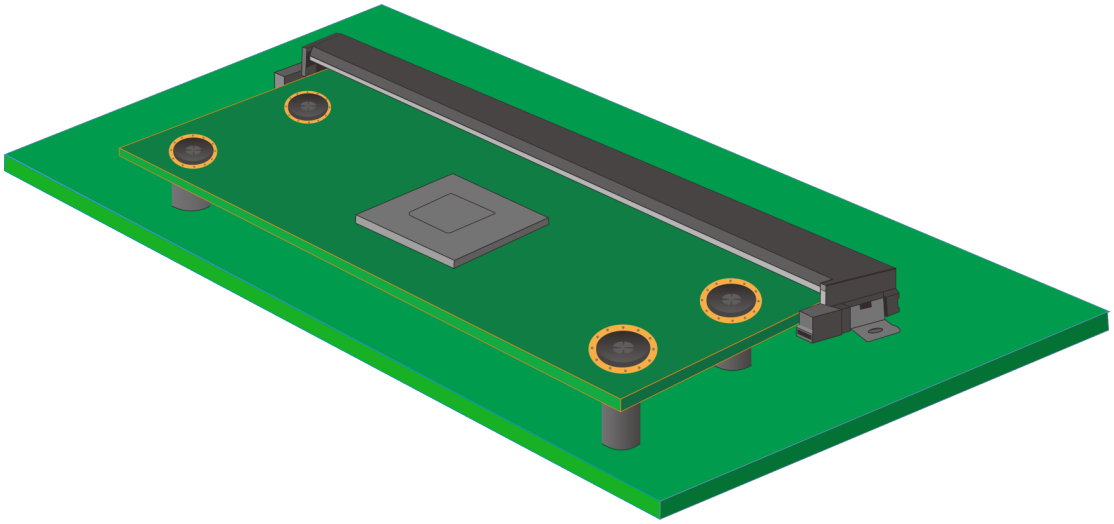


Figure 19 Screw Fixation

Standoffs secured to the Carrier board are expected. The standoffs are to be used with M2.5 hardware. Most implementations will use Carrier board standoffs that have M2.5 threads (as opposed to clearance holes). A short M2.5 screw and washer, inserted from the Module top side, secures the Module to the Carrier board threaded standoff.

The *SMARC* connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer

for the 5mm stack would likely be a standard length.

Penn Engineering and Manufacturing (PEM) (www.pemnet.com) makes surface mount spacers with M2.5 internal threads. The product line is called SMTSO ("surface mount technology stand offs"). The shortest standard length offered is 2mm. A custom part with 1.5mm standoff length, M2.5 internal thread, and 5.56mm standoff OD is available from PEM. The Carrier PCB requires a 4.22mm hole and 6.2mm pad to accept these parts.

Other vendors such as RAF Electronic Hardware (www.rafhdwe.com) offer M2.5 compatible swaged standoffs. Swaged standoffs require the use of a press and anvil at the CM. Their use is common in the industry. The standoff OD and Carrier PCB hole size requirements are different from the PEM SMTSO standoffs described above.

2.3.8. Carrier Connector

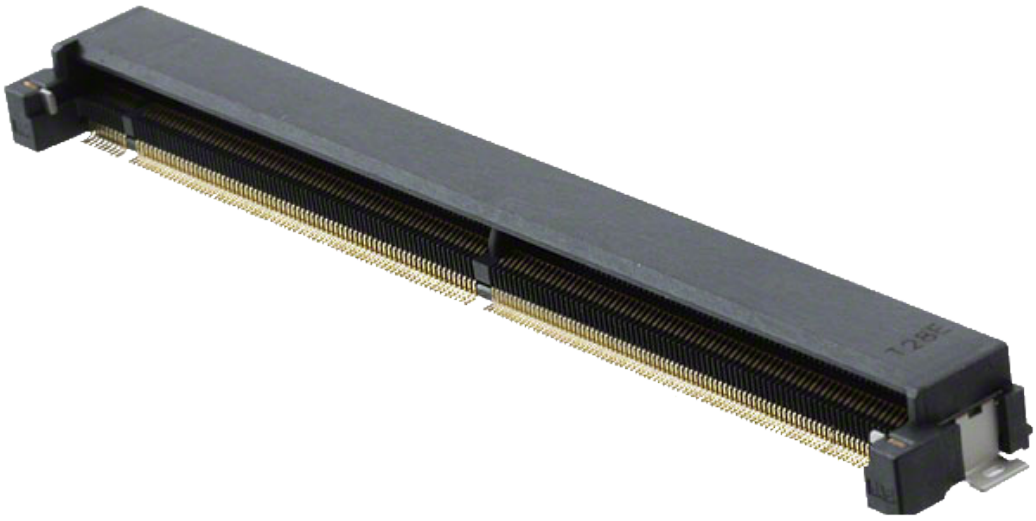


Figure 20 MXM3 Carrier Connector

The Carrier board connector is a 314 pin 0.5mm pitch right angle part designed for use with 1.2mm thick mating PCBs with the appropriate edge finger pattern. The connector is commonly used for MXM3 graphics cards. The *SMARC* Module uses the connector in a way quite different from the *MXM3* usage.

Vender	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color
Foxconn	AS0B821-S43B - *H	1.5mm	4.3mm	Flash	Std	Black
Foxconn	AS0B821-S43N - *H	1.5mm	4.3mm	Flash	Std	Ivory
Foxconn	AS0B826-S43B - *H	1.5mm	4.3mm	10 u-in	Std	Black
Foxconn	AS0B826-S43N - *H	1.5mm	4.3mm	10 u-in	Std	Ivory
Lotes	AAA-MXM-008-P04_A	1.5mm	4.3mm	Flash	Std	Tan
Lotes	AAA-MXM-008-P03	1.5mm	4.3mm	15 u-in	Std	Tan
Speedtech	B35P101-02111-H	1.56mm	4.0mm	Flash	Std	Black
Speedtech	B35P101-02011-H	1.56mm	4.0mm	Flash	Std	Tan
Speedtech	B35P101-02112-H	1.56mm	4.0mm	10 u-in	Std	Black
Speedtech	B35P101-02012-H	1.56mm	4.0mm	10 u-in	Std	Tan
Speedtech	B35P101-02113-H	1.56mm	4.0mm	15 u-in	Std	Black
Speedtech	B35P101-02013-H	1.56mm	4.0mm	15 u-in	Std	Tan
Aces	91781-314 2 8-001	2.7mm	5.2mm	3 u-in	Std	Black

Vender	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color
Foxconn	AS0B821-S55B - *H	2.7mm	5.5mm	Flash	Std	Black
Foxconn	AS0B821-S55N - *H	2.7mm	5.5mm	Flash	Std	Ivory
Foxconn	AS0B826-S55B - *H	2.7mm	5.5mm	10 u-in	Std	Black
Foxconn	AS0B826-S55N - *H	2.7mm	5.5mm	10 u-in	Std	Ivory
Speedtech	B35P101-02121-H	2.76mm	5.2mm	Flash	Std	Black
Speedtech	B35P101-02021-H	2.76mm	5.2mm	Flash	Std	Tan
Speedtech	B35P101-02122-H	2.76mm	5.2mm	10 u-in	Std	Black
Speedtech	B35P101-02022-H	2.76mm	5.2mm	10 u-in	Std	Tan
Speedtech	B35P101-02123-H	2.76mm	5.2mm	15 u-in	Std	Black
Speedtech	B35P101-02023-H	2.76mm	5.2mm	15 u-in	Std	Tan
Foxconn	AS0B821-S78B - *H	5.0mm	7.8	Flash	Std	Black
Foxconn	AS0B821-S78N - *H	5.0mm	7.8	Flash	Std	Ivory
Foxconn	AS0B826-S78B - *H	5.0mm	7.8	10 u-in	Std	Black
Foxconn	AS0B826-S78N - *H	5.0mm	7.8	10 u-in	Std	Ivory
Yamaichi (1)	CN113-314-2001	5.0mm	7.8	0.3 u-meter	Std	Black

Other, taller stack heights may be available from these and other vendors. Stack heights as tall as 11mm are shown on the Aces web site.

Note:

1. *Yamaichi CN113-314-2001* is automotive grade.
2. The vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for *SMARC* use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The *SMARC* module "ungangs" these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to *SMARC* is given in the sections below.

2.3.9. Module Cooling Solution—Heat Spreader

A standard heat-spreader plate for use with the *SMARC* 82mm x 50mm form factor is described below. A standard heat spreader plate definition allows the customer to use a Module from multiple vendors.

The heat spreader plate is sized at 82mm x 42mm x 3mm, and sits 3mm above the *SMARC* Module. The heat spreader plate 'Y' dimension is deliberately set at 42mm and not 50mm, to allow the plate to clear the *SMARC MXM3* connector. The plate is shown in the figures below.

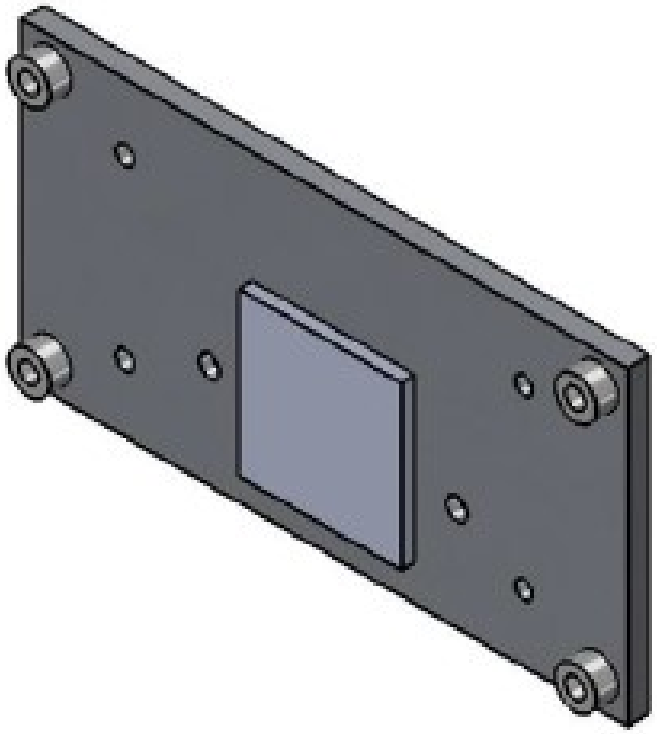


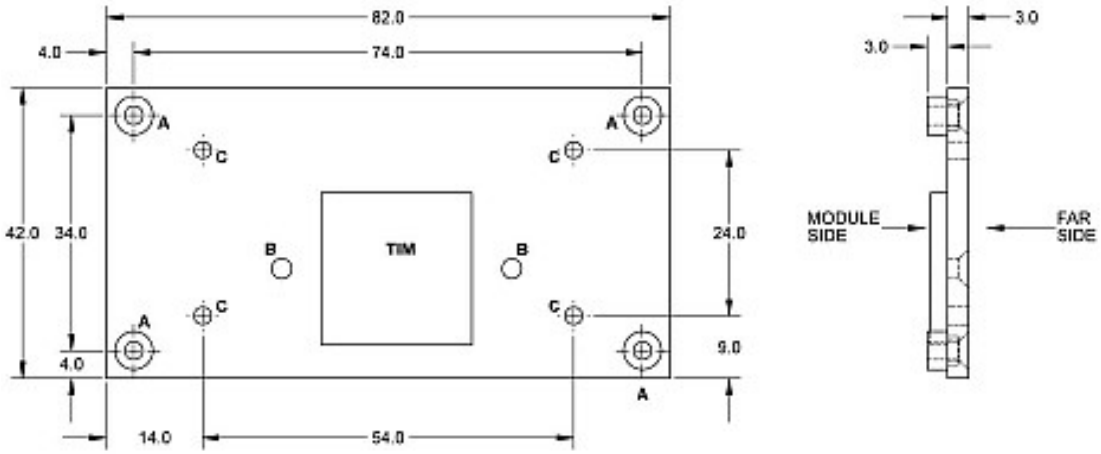
Figure 21 Heat Spreader

The internal square in the figure above is a thermally conductive and mechanically compliant Thermal Interface Material (or "TIM"). The exact X-Y position and Z thickness details of the TIM vary from design to design.

The two holes immediately adjacent to the TIM serve to secure the PCB in the SOC area and compress the TIM.

The four interior holes that are further from the center allow a heat sink to be attached to the heat spreader plate, or they can be used to secure the heat spreader plate to a chassis wall that serves as a heat sink.

Dimensions and further details may be found in the following figure.



Dimensions in the figure above are in millimeters. “TIM” stands for “Thermal Interface Material”. The TIM takes up the small gap between the SOC top and the Module - facing side of the heat spreader.

Hole Reference	Description	Size
A	SMARC Module corner mounting holes Spacing determined by SMARC specification for 82mm x 50mm Modules. Typically these holes have 3mm length press fit or swaged clearance standoffs on the Module side. These holes are typically countersunk on the far side of the plate, to allow the heat spreader plate to be flush with a secondary heat sink.	Hole size depends on standoffs used. Standoff diameter must be compatible with SMARC Module mounting hole pad and hole size (6.0mm pads, 2.7mm holes on the Module). The holes and standoffs are for use with M2.5 screw hardware. The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
B	Not Defined	
C	Fixed location holes to allow the attachment of a heat sink to the heat spreader, or to allow the heat spreader to be secured to a chassis wall that can serve as a heat sink.	M3 threaded holes

2.4 Electrical Specifications

2.4.1. Supply Voltage

The *SMARC-iMX93* module operates over an input voltage range of 3.0V to 5.25V. Power is provided from the carrier through 10 power pins as defined by the *SMARC* specification.

Caution! A single 5V or 3.3V DC input is recommended.

2.4.2. RTC/Backup Voltage

3.0V RTC backup power is provided through the VDD_RTC pin from the carrier board. This connection provides back up power to the module PMIC. The RTC is powered via the primary system 3.3V supply during normal operation and via the VBAT power input, if it is present, during power-off.

2.4.3. No Separate Standby Voltage

The *SMARC-iMX93* does not have a standby power rail. Standby operation is powered through the main supply voltage rail, as defined in the *SMARC* specification.

2.4.4. Module I/O Voltage

The *SMARC-iMX93* module supports 1.8V (*SMARC* v2.0 compliant) level I/O voltage depending on the part number that users selected.

2.4.5. MTBF

The *SMARC-iMX93* System *MTBF* (hours) : >100,000 hours

The above *MTBF* (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50°C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40°C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

2.4.6. Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes an *SMARC-iMX93* module, carrier board is *EVK-STD-CARRIER-S20* with *7-inch* LVDS display, SD card and USB keyboard. The carrier board was powered externally by a power supply unit so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. The modules were cooled by the heatspreader specific to the module variants.

Each module was measured while running Yocto Sumo. To measure the worst case power consumption, the cooling solution was removed and the CPU core temperature was allowed to run between 95° and 100°C at 100% workload. The peak current value was then recorded. This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:
Yocto Mickledore

• Desktop Idle
• 100% CPU workload

Note: With the linux stress tool, we stressed the CPU to maximum frequency.
The table below provides additional information about the different variants offered by the *SMARC-iMX93*.

SMARC Part Number	*Desktop Idle*	*100% workload*
SMARC-iMX93-2G-I	*TBD*	*2.1W*

2.5 Environmental Specifications

2.5.1. Operating Temperature

The *SMARC-iMX93* module operates from -40°C to 85°C air temperature, with a passive heat sink arrangement.

2.5.2. Humidity

Operating: 10% to 90% RH (non-condensing).
Non-operating: 5% to 95% RH (non-condensing).

2.5.3. ROHS/REACH Compliance

The *SMARC-iMX93* module is compliant to the *2002/95/EC RoHS* directive and *REACH* directive.

Connector PinOut

This Chapter gives detail pinout of *SMARC-iMX93* golden finger edge connector.

Section include：

- *SMARC-iMX93* Connector Pin Mapping

Chapter 3 Connector Pinout

The Module pins are designated as *P1 – P156* on the Module Primary (Top) side, and *S1 – S158* on the Module Secondary (Bottom) side. There are total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used.

The *SMARC-iMX93* module pins are deliberately numbered as *P1 – P156* and *S1 – S158* for clarity and to differentiate the *SMARC* Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use different pin numbering scheme.

3.1 SMARC-iMX93 Connector Pin Mapping

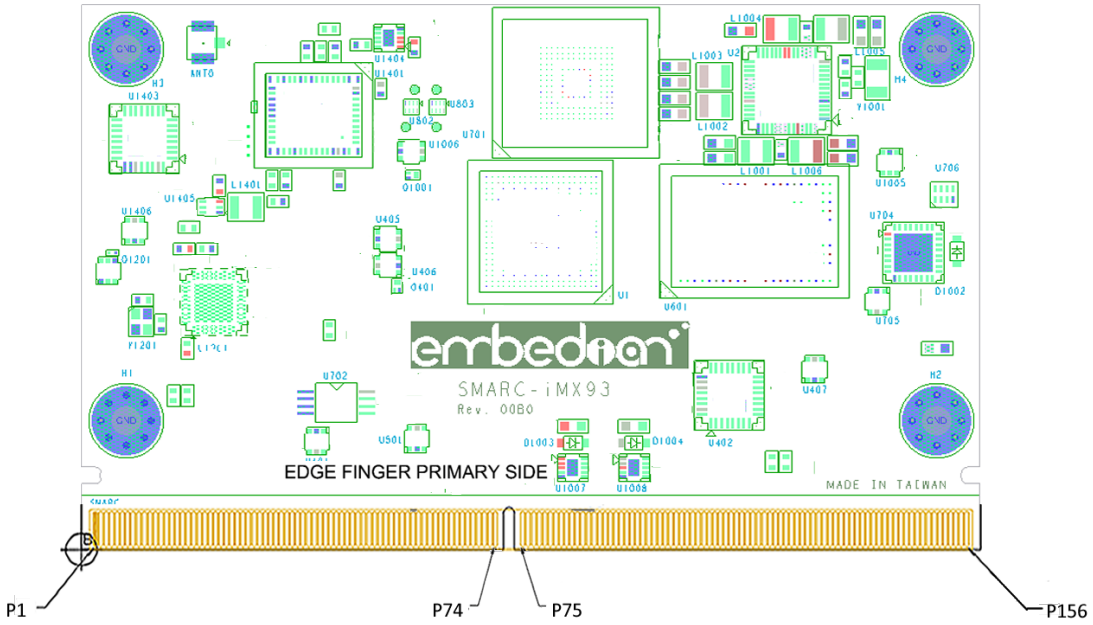


Figure 22 SMARC-iMX93 edge finger primary pins

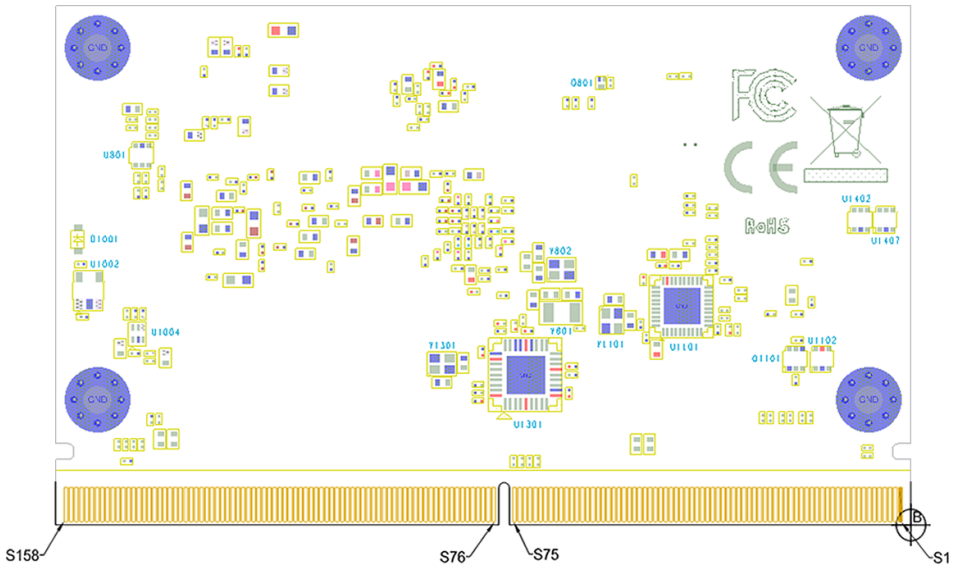


Figure 23 SMARC-iMX93 edge finger secondary pins

The next tables describe each pin, its properties, and its use on the module and development board.

The "*SMARC Edge Finger*" column shows the connection of the signals defined in the *SMARC* specification. The "*NXP i.MX93 CPU*" column shows the connection of the CPU signals on the module. The format of this column is "*Ball/Mode/Signal Name*" where "*Signal Name*" is the chip where the signals are connected, and "*Ball*" is the name of the pad where the signals are connected as they are defined in the *i.MX93* processor datasheet.

Pinout Legend

I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P1	SMB_ALERT_1V8#					Not used
P2	GND				P	Ground
P3	CSI1_CK+					Not used
P4	CSI1_CK-					Not used
P5	GBE1_SDP					Not used
P6	GBE0_SDP					Not used
P7	CSI1_RX0+					Not used
P8	CSI1_RX0-					Not used
P9	GND				P	Ground
P10	CSI1_RX1+					Not used
P11	CSI1_RX1-					Not used
P12	GND				P	Ground
P13	CSI1_RX2+					Not used
P14	CSI1_RX2-					Not used
P15	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P16	CSI1_RX3+					Not used
P17	CSI1_RX3-					Not used
P18	GND				P	Ground
P19	GbE0_MDI3-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 3
P20	GbE0_MDI3+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 3
P21	GbE0_LINK100#				O OD	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
P22	GbE0_LINK1000#				O OD	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current
P23	GbE0_MDI2-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 2
P24	GbE0_MDI2+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 2

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P25	GbE0_LINK_ACT#				O OD	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
P26	GbE0_MDI1-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 1
P27	GbE0_MDI1+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 1
P28	GbE0_CTREF					Not used
P29	GbE0_MDI0-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 0
P30	GbE0_MDI0+				AIO	Realtek RTL8211FD-CG: Differential Transmit/Receive Positive Channel 0

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P31	SPI0_CS1#	Port 16 of i2c GPIO expander A			O	SPI0 Master Chip Select 1 output.
P32	GND				P	Ground
P33	SDIO_WP	Port 10 of i2c GPIO expander A			I	Write Protect
P34	SDIO_CMD	Y19	ALT0	SD2_CMD__ USDHC2_CMD	IO	Command Line
P35	SDIO_CD#	Y17	ALT5	SD2_CD_B__ GPIO3_IO00	I	Card Detect
P36	SDIO_CK	AA19	ALT0	SD2_CLK__ USDHC2_CLK	O	Clock
P37	SDIO_PWR_EN	AA17	ALT5	SD2_RESET_B__ GPIO2_IO19	O	SD card power enable
P38	GND				P	Ground
P39	SDIO_D0	Y18	ALT0	SD2_DATA0__ USDHC2_DATA0	IO	Data path
P40	SDIO_D1	AA18	ALT0	SD2_DATA1__ USDHC2_DATA1	IO	Data path
P41	SDIO_D2	Y20	ALT0	SD2_DATA2__ USDHC2_DATA2	IO	Data path
P42	SDIO_D3	AA20	ALT0	SD2_DATA3__ USDHC2_DATA3	IO	Data path

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P43	SPI0_CS0#	M20	ALT0	GPIO_IO08__ GPIO2_IO08	O	SPI0 Master Chip Select 0 output,
P44	SPI0_CK	N18	ALT1	GPIO_IO11__ LPSPI3_SCK	O	SPI0 Master Clock output
P45	SPI0_DIN	M21	ALT1	GPIO_IO09__ LPSPI3_SIN	I	SPI0 Master Data input (input to CPU, output from SPI device)
P46	SPI0_DO	N17	ALT1	GPIO_IO10__ LPSPI3_SOUT	O	SPI0 Master Data output (output from CPU, input to SPI device)
P47	GND				P	Ground
P48	SATA_TX+					Not used
P49	SATA_TX-					Not used
P50	GND				P	Ground
P51	SATA_RX+					Not used
P52	SATA_RX-					Not used
P53	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P54	ESPI_CS0#/ SPI1_CS0#	J21	ALT0	GPIO_IO00__ GPIO2_IO00	O	SPI1 Master Chip Select 0 output
P55	ESPI_CS1#/ SPI1_CS1#	Port 17 of i2c GPIO expander A			O	SPI1 Master Chip Select 1 output
P56	ESPI_CK/ SPI1_CK	K21	ALT4	GPIO_IO03__ LPSPI6_SCK	O	SPI1 Master Clock output
P57	ESPI_IO_1/ SPI1_DIN	J20	ALT4	GPIO_IO01__ LPSPI6_SIN	I	SPI1 Master Data input (input to CPU, output from SPI device)
P58	ESPI_IO_0/ SPI1_DO	K20	ALT4	GPIO_IO02__ LPSPI6_SOUT	O	SPI1 Master Data output (output from CPU, input to SPI device)
P59	GND				P	Ground
P60	USB0+	B14		USB1_D_P	AIO	Differential USB0 data
P61	USB0-	A14		USB1_D_N	AIO	Differential USB0 data
P62	USB0_EN_OC#	Port 18 (USB_EN) and Port 19 (USB_OC#) of i2c IO expander A			IO OD	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P63	USB0_VBUS_DET	F12		USB_OTG_VBUS	I	USB host power detection, when this port is used as a device
P64	USB0_OTG_ID	C11		USB1_ID	I	USB OTG ID input, active high
P65	USB1+				IO	Differential USB1 data pair (from USB2514 port 3)
P66	USB1-				IO	Differential USB1 data pair (from USB2514 port 3)
P67	USB1_EN_OC#	From USB2514			IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier
P68	GND				P	Ground
P69	USB2+				IO	Differential USB2 data pair (from USB2514 port2)
P70	USB2-				IO	Differential USB2 data pair (from USB2514 port2)

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P71	USB2_EN_OC#	From USB2514			IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier
P72	RSVD					Not used
P73	RSVD					Not used
P74	USB3_EN_OC#	From USB2514			IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P75	PCIE_A_RST#					Not used
P76	USB4_EN_OC#	From USB2514				Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier
P77	PCIE_B_CKREQ#					Not used
P78	PCIE_A_CKREQ#					
P79	GND				P	Ground
P80	PCIE_C_REFCK+					Not used
P81	PCIE_C_REFCK-					Not used
P82	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P83	PCIE_A_REFCK+					Not used
P84	PCIE_A_REFCK-					Not used
P85	GND				P	
P86	PCIE_A_RX+					Not used
P87	PCIE_A_RX-					Not used
P88	GND				P	Ground
P89	PCIE_A_TX+					Not used
P90	PCIE_A_TX-					Not used
P91	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P92	HDMI_D2+ / DP1_LANE0+					Not used
P93	HDMI_D2- / DP1_LANE0-					Not used
P94	GND				P	Ground
P95	HDMI_D1+/ DP1_LANE1+					Not used
P96	HDMI_D1-/ DP1_LANE1-					Not used
P97	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P98	HDMI_D0+/ DP1_LANE2+					Not used
P99	HDMI_D0-/ DP1_LANE2-					Not used
P100	GND				P	Ground
P101	HDMI_CK+/ DP1_LANE3+					Not used
P102	HDMI_CK-/ DP1_LANE3-					Not used
P103	GND				P	Ground
P104	HDMI_HPD/ DP1_HDP					Not used
P105	HDMI_CTRL_CK / DP1_AUX+					Not used
P106	HDMI_CTRL_DAT/ DP1_AUX-					Not used
P107	DP1_AUX_SEL					Not used

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P108	GPIO0 / CAM0_PWR#	Port 0 of i2c GPIO expander B			IO	Camera 0 Power Enable, active low output
P109	GPIO1 / CAM1_PWR#	Port 1 of i2c GPIO expander B			IO	Camera 1 Power Enable, active low output
P110	GPIO2 / CAM0_RST#	Port 2 of i2c GPIO expander B			IO	Camera 0 Reset, active low output
P111	GPIO3 / CAM1_RST#	Port 3 of i2c GPIO expander B			IO	Camera 1 Reset, active low output
P112	GPIO4 / HDA_RST#	Port 4 of i2c GPIO expander B			IO	HD Audio Reset, active low output
P113	GPIO5 / PWM_OUT	G18	ALT5 ALT3	PDM_BIT_STREAM1__GPIO01_IO10 /TPM2_EXTCLK	IO	PWM output
P114	GPIO6 / TACHIN	Port 5 of i2c GPIO expander			IO	Tachometer input (used with the GPIO5 PWM)
P115	GPIO7	Port 6 of i2c GPIO expander			IO	
P116	GPIO8	Port 7 of i2c GPIO expander			IO	
P117	GPIO9	Port 8 of i2c GPIO expander			IO	
P118	GPIO10	Port 9 of i2c GPIO expander			IO	
P119	GPIO11	Port 10 of i2c GPIO expander			IO	
P120	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P121	I2C_PM_CK	D20	ALT0	I2C2_SCL__ LPI2C2_SCL	IO OD	Power management I2C bus clock
P122	I2C_PM_DAT	D21	ALT0	I2C2_SDA__ LPI2C2_SDA	IO OD	Power management I2C bus data
P123	BOOT_SEL0#	B4	ALT0	GPIO1_IO05__ GPIO1_IO05	I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P124	BOOT_SEL1#	A3	ALT0	GPIO1_IO06__ GPIO1_IO06	I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P125	BOOT_SEL2#	F6	ALT0	GPIO1_IO07__ GPIO1_IO07	I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P126	RESET_OUT#				O	General purpose reset output to Carrier board.

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P127	RESET_IN#				I	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise Pulled up on Module. Driven by OD part on Carrier.
P128	POWER_BTN#				I	Power-button input from carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
P129	SER0_TX	L17	ALT5	GPIO_IO04__ LPUART6_TX	O	Asynchronous serial port data out
P130	SER0_RX	L18	ALT5	GPIO_IO05__ LPUART6_RX	I	Asynchronous serial port data in
P131	SER0_RTS#	L20	ALT5	GPIO_IO06__ LPUART6_CTS_B	O	Request to Send handshake line for SER0
P132	SER0_CTS#	L21	ALT5	GPIO_IO07__ LPUART6_RTS_B	I	Clear to Send handshake line for SER0
P133	GND				P	Ground
P134	SER1_TX	F21	ALT0	UART2_TXD__ LPUART2_TX	O	Asynchronous serial port data out
P135	SER1_RX	F20	ALT0	UART2_RXD__ LPUART2_RX	I	Asynchronous serial port data in

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P136	SER2_TX	N20	ALT5	GPIO_IO12__ LPUART8_TX		Asynchronous serial port data out
P137	SER2_RX	N21	ALT5	GPIO_IO13__ LPUART8_RX		Asynchronous serial port data in
P138	SER2_RTS#	P21	ALT5	GPIO_IO15__ LPUART8_RTS_B		Request to Send handshake line for SER2
P139	SER2_CTS#	P20	ALT5	GPIO_IO14__ LPUART8_CTS_B		Clear to Send handshake line for SER2
P140	SER3_TX	E21	ALT0	UART1_TXD__ LPUART1_TX	O	Asynchronous serial port data out
P141	SER3_RX	E20	ALT0	UART1_RXD__ LPUART1_RX	I	Asynchronous serial port data in
P142	GND				P	Ground
P143	CAN0_TX	G17	ALT6	PDM_CLK__ CAN1_TX	O	CAN0 Transmit output
P144	CAN0_RX	J17	ALT6	PDM_BIT_STREAM0__ CAN1_RX	I	CAN0 Receive input
P145	CAN1_TX	V21	ALT2	GPIO_IO25__ CAN2_TX	O	CAN1 Transmit output
P146	CAN1_RX	W21	ALT2	GPIO_IO27__ CAN2_RX	I	CAN1 Receive input

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P147	VDD_IN				P	Power in
P148	VDD_IN				P	Power in
P149	VDD_IN				P	Power in
P150	VDD_IN				P	Power in
P151	VDD_IN				P	Power in
P152	VDD_IN				P	Power in
P153	VDD_IN				P	Power in
P154	VDD_IN				P	Power in
P155	VDD_IN				P	Power in
P156	VDD_IN				P	Power in

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S1	CSI1_TX+/ I2C_CAM1_CK					Not used
S2	CSI1_TX-/ I2C_CAM1_DAT					Not used
S3	GND				P	Ground
S4	RSVD					Not used
S5	CSI0_TX+ / I2C_CAM0_CK	C20	ALT0	I2C1_SCL__ LPI2C1_SCL	IO OD	Camera0 I2C bus clock
S6	CAM_MCK	U4	ALT0	CCM_CLKO3__ CCMSRCGPCMIX_ CLKO3	O	Master clock output for CSI camera support
S7	CSI0_TX- / I2C_CAM0_DAT	C21	ALT0	I2C1_SDA__ LPI2C1_SDA	IO OD	Camera0 I2C bus data
S8	CSI0_CK+	E10		MIPI_CSI1_CLK_P	I	CSI0 differential clock inputs
S9	CSI0_CK-	D10		MIPI_CSI1_CLK_N	I	CSI0 differential clock inputs
S10	GND				P	Ground
S11	CSI0_RX0+	B11		MIPI_CSI1_D0_P	I	CS0 differential data inputs 0+
S12	CSI0_RX0-	A11		MIPI_CSI1_D0_N	I	CSI0 differential data input 0-
S13	GND				P	Ground
S14	CSI0_RX1+	B10		MIPI_CSI1_D1_P	I	CSI0 differential data input 1+
S15	CSI0_RX1-	A10		MIPI_CSI1_D1_N	I	CSI0 differential data inputs 1-
S16	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S17	GbE1_MDI0+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 0
S18	GbE1_MDI0-				AIO	Realtek RTL8211FD-CG: Differential Transmit/Receive Negative Channel 0
S19	GbE1_LINK100#				O OD	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
S20	GbE1_MDI1+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 1
S21	GbE1_MDI1-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 1
S22	GbE1_LINK1000#				O OD	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S23	GbE1_MDI2+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 2
S24	GbE1_MDI2-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 2
S25	GND				P	Ground
S26	GbE1_MDI3+				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Positive Channel 3
S27	GbE1_MDI3-				AIO	Realtek RTL8211FD-CG Differential Transmit/Receive Negative Channel 3
S28	GbE1_CTREF					Not used
S29	PCIE_D_TX+					Not used
S30	PCIE_D_TX-					Not used
S31	GBE1_LINK_ACK#				O OD	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
S32	PCIE_D_RX+					Not used
S33	PCIE_D_RX-					Not used
S34	GND					Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S35	USB4+					Differential USB4 data pair (from USB2514 port 4)
S36	USB4-					Differential USB4 data pair (from USB2514 port 4)
S37	USB3_VBUS_DET					Not used
S38	AUDIO_MCK	R20	ALT1	GPIO_IO17__ SAI3_MCLK	O	Master clock output to Audio codecs
S39	I2S0_LRCK	V20	ALT7	GPIO_IO26__S AI3_TX_SYNC	IO	Left& Right audio synchronization clock
S40	I2S0_SDOUT	R17	ALT7	GPIO_IO19__ SAI3_TX_DATA 00	O	Digital audio Output
S41	I2S0_SDIN	T20	ALT1	GPIO_IO20__ SAI3_RX_DAT A00	I	Digital audio Input
S42	I2S0_CK	R21	ALT1	GPIO_IO16__S AI3_TX_BCLK	IO	Digital audio clock
S43	ESPI_ALERT0#					Not used
S44	ESPI_ALERT1#					Not used
S45	RSVD					Not used
S46	RSVD					Not used
S47	GND				G	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S48	I2C_GP_CK	Y21	ALT11	GPIO_IO29__ LPI2C3_SCL	IO OD	General purpose I2C bus clock
S49	I2C_GP_DAT	W20	ALT11	GPIO_IO28__ LPI2C3_SDA	IO OD	General purpose I2C bus clock
S50	HDA_SYNC/ I2S2_LRCK	G21	ALT0	SAI1_TXFS__ SAI1_TX_SYNC	IO	Left& Right audio synchronization clock
S51	HDA_SDO/ I2S2_SDOUT	H21	ALT0	SAI1_TXD0__ SAI1_TX_DATA00	O	Digital audio Output
S52	HDA_SDI/ I2S2_SDIN	H20	ALT0	SAI1_RXD0__SAI1_ RX_DATA00	I	Digital audio Input
S53	HDA_CK/ I2S2_CK	G20	ALT0	SAI1_TXC__ SAI1_TX_BCLK	IO	Digital audio clock
S54	SATA_ACT#					Not used
S55	USB5_EN_OC#					Not used
S56	ESPI_IO_2					Not used
S57	ESPI_IO_3					Not used
S58	ESPI_RESET#					Not used
S59	USB5+					Not used
S60	USB5-					Not used
S61	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S62	USB3_SSTX+					Not used
S63	USB3_SSTX-					Not used
S64	GND				P	Ground
S65	USB3_SSRX+					Not used
S66	USB3_SSRX-					Not used
S67	GND				P	Ground
S68	USB3+					Differential USB3 data pair (from USB2514 port 1)
S69	USB3-					Differential USB3 data pair (from USB2514 port 1)
S70	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S71	USB2_SSTX+					Not used
S72	USB2_SSTX--					Not used
S73	GND				P	Ground
S74	USB2_SSRX+					Not used
S75	USB2_SSRX-					Not used
S76	PCIE_B_RST#					Not used
S77	PCIE_C_RST#					Not used
S78	PCIE_C_RX+					Not used
S79	PCIE_C_RX-					Not used
S80	GND				P	Ground
S81	PCIE_C_TX+					Not used
S82	PCIE_C_TX-					Not used
S83	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S84	PCIE_B_REFCK+					Not used
S85	PCIE_B_REFCK-					Not used
S86	GND				P	Ground
S87	PCIE_B_RX+					Not used
S88	PCIE_B_RX-					Not used
S89	GND				P	Ground
S90	PCIE_B_TX+					Not used
S91	PCIE_B_TX-					Not used
S92	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S93	DP0_LANE0+				AIO	eDP0 data pair 0+
S94	DP0_LANE0-				AIO	eDP0 data pair 0-
S95	DP0_AUX_SEL					Not used
S96	DP0_LANE1+				AIO	eDP0 data pair 1+
S97	DP0_LANE1-				AIO	eDP0 data pair 1-
S98	DP0_HPD				I	eDP 0 Hot Plug Detect pins
S99	DP0_LANE2+				AIO	eDP0 data pair 2+
S100	DP0_LAN2-				AIO	eDP0 data pair 2-
S101	GND				P	Ground
S102	DP0_LANE3+				AIO	eDP0 data pair 3+
S103	DP0_LANE3-				AIO	eDP0 data pair 3-

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S104	USB3_OTG_ ID					Not used
S105	DP0_AUX+					eDP0 auxiliary channel pair +
S106	DP0_AUX-					eDP0 auxiliary channel pair -
S107	LCD1_BKLT_EN	Port 23 of i2c GPIO Expander A			O	High enables lvds1 panel backlight
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	A18	N/A	MIPI_DSI1_CLK_P	O	LVDS1/eDP1/DSI1 LCD differential clock pairs
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	B18	N/A	MIPI_DSI1_CLK_N	O	LVDS1/eDP1/DSI1 LCD differential clock pairs
S110	GND				P	Ground
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	A16	N/A	MIPI_DSI1_D0_P	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 1
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	B16	N/A	MIPI_DSI1_D0_N	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 1
S113	eDP1_HPD					Not used

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	A17	N/A	MIPI_DSI1_D1_P	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 2
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	B17	N/A	MIPI_DSI1_D1_N	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 2
S116	LCD1_VDD_EN	D8	ALT0	GPIO1_GPIO11__ GPIO1_IO11	O	High enables lvds1 panel VDD
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	A19	N/A	MIPI_DSI1_D2_P	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 3
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	B19	N/A	MIPI_DSI1_D2_ N	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 3
S119	GND				P	Ground
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	A20	N/A	MIPI_DSI1_D3_P	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 4
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	B20	N/A	MIPI_DSI1_D3_ N	AIO	LVDS1/eDP1/DSI1 LCD data channel differential pairs 4
S122	LCD1_BKLT_ PWM	T21	ALT6	GPIO_IO21__ TPM4_CH1	O	LCD1 display backlight PWM control
S123	GPIO13	Port 12 of i2c GPIO expander B				GPIO13
S124	GND				P	Ground

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	B5	N/A	LVDS_D0_P	AIO	LVDS0 LCD data channel differential pairs 1
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	A5	N/A	LVDS_D0_N	AIO	LVDS0 LCD data channel differential pairs 1
S127	LCD_BKLT_EN	Port 21 of i2c GPIO Expander A			O	High enables lvds0 panel backlight
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	B4	N/A	LVDS_D1_P	AIO	LVDS0 LCD data channel differential pairs 2
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	A4	N/A	LVDS_D1_N	AIO	LVDS0 LCD data channel differential pairs 2
S130	GND				P	Ground
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	B2	N/A	LVDS_D2_P	AIO	LVDS0 LCD data channel differential pairs 3
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	A2	N/A	LVDS_D2_N	AIO	LVDS0 LCD data channel differential pairs 3

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S133	LCD_VDD_EN	Port 20 of i2c GPIO Expander A			O	High enables lvds0 panel VDD
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	B3	N/A	LVDS_CLK_P	O	LVDS0 LCD differential clock pairs
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	A3	N/A	LVDS_CLK_N	O	LVDS0 LCD differential clock pairs
S136	GND				P	Ground
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	C1	N/A	LVDS_D3_P	AIO	LVDS0 LCD data channel differential pairs 4
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	B1	N/A	LVDS_TX3_N	AIO	LVDS0 LCD data channel differential pairs 4
S139	I2C_LCD_CK	U20	ALT11	GPIO_IO23__ LPI2C5_SCL	IO OD	LCD display I2C bus clock
S140	I2C_LCD_DAT	AE8	ATL0	LVDS1_I2C0_SDA__ LVDS1_I2C0_SDA	IO OD	LCD display I2C bus clock
S141	LCD_BKLT_PWM	U21	ALT4	GPIO_IO24__ TPM3_CH3	O	LCD0 display backlight PWM control
S142	GPIO12	A8	ALT0	GPIO1_IO08__ GPIO1_IO08		GPIO
S143	GND				P	Ground
S144	eDP0_HPD					Not used
S145	WDT_TIME_OUT#	Y3	ALT5	CCM_CLKO2__ GPIO3_IO27	O	Watchdog-Timer Output

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S146	PCIE_WAKE#				I	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.
S147	VDD_RTC				P	Low current RTC circuit backup power - 3.0V nominal It is sourced from a Carrier based Lithium cell or Super Cap
S148	LID#	From Port0 of PCAL6408APWJ IO Expander			I	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		NXP i.MX93 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S149	SLEEP#	From Port1 of PCAL6408APWJ IO Expander			I	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.
S150	VIN_PWR_BAD#				I	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		NXP i.MX93MQ CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S151	CHARGING#	From Port2 of PCAL6408APWJ IO Expander			I	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.
S152	CHARGER_PRSNT#	From Port4 of PCAL6408APWJ IO Expander			I	Held low by Carrier if DC input for battery charger is present.
S153	CARRIER_STBY#				O	The Module shall drive this signal low when the system is in a standby power state
S154	CARRIER_PWR_ON				O	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.
S155	FORCE_RECOV#				I	Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		NXP i.MX93MQ CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S156	BATLOW#	From Port3 of PCAL6408APWJ IO Expander			I	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.
S157	TEST#				I	Held low by Carrier to invoke Module SD Boot UP. Pulled up on Module. Driven by OD part on Carrier.
S158	GND				P	Ground

Power Control Signals between SMARC Module and Carrier

This Chapter points out the handshaking rule between *SMARC* module and carrier.
Section include：

- *SMARC-iMX93* Module Power
- Power Signals
- Power Flow and Control Signals Block Diagram
- Power States
- Power Sequences
- Terminations
- Boot Select

Chapter 4 Power Control Signals between SMARC-iMX93 Module and Carrier

SMARC modules are designed to be driven with a single +3V to +5.25V input power rail. Unlike Q7 module, there is no separate voltage rail for standby power, other than the very low current RTC voltage rail. All module operating and standby power comes from the single set of *VDD_IN* pins. This suits battery power sources well, and is also easy to use with non-battery sources.

SMARC module has specific handshaking rules to the carrier by *SMARC* hardware specification. To design the carrier board, users need to follow these rules or it might not boot up. Some pull-up and pull-down also need to be cared to make all functions work.

4.1 SMARC-iMX93 Module Power

4.1.1. Input Voltage / Main Power Rail

The allowable Module DC input voltage range for *SMARC-iMX93* is from 3.0V to 5.25V. This voltage is brought in on the *VDD_IN* pins and returned through the numerous *GND* pins on the connector.

Ten pins are allocated to *VDD_IN*. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage, this would allow up to 16.75W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 10W may be brought in at 3V.
SMARC-iMX93 typically consumes 2~4W and is pretty safe in using the connector.

4.1.2. No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low current RTC voltage rail. *SMARC-iMX93* operating and standby power comes from the single set of *VDD_IN* pins. This suits battery power sources well, and is also easy to use with non-battery sources.

4.1.3. RTC/Backup Voltage

RTC backup power is brought in on the *VDD_RTC* rail. The RTC consumption is typically 15 microA or less. The allowable *VDD_RTC* voltage range shall be 2.0V to 3.25V. The *VDD_RTC* rail is sourced from a Carrier based Lithium cell, or it may be left open if the RTC backup functions are not required. *SMARC-iMX93* module is able to boot without a *VDD_RTC* voltage source.

Lithium cells, if used on Carrier, shall be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module *VDD_RTC* side.

Note that if a Super cap is used, current may flow out of the Module *VDD_RTC* rail to charge the Super Cap.

4.1.4. Power Sequencing

The Module signal *CARRIER_PWR_ON* exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits should not be powered until the Module asserts the *CARRIER_PWR_ON* signal as a high. Module hardware will assert *CARRIER_PWR_ON* when all Module supplies necessary for Module booting are up.

The IO power of carrier board will be turn on at the stage of power on sequence. If the IO power of carrier board been turn on earlier than the *SMARC* module, the

power on carrier board might feedback to *SMARC* module through IO lines and disturbs the *SMARC* module power on sequence. More seriously, it might cause to the CPU won't boot up. It is always recommended that the power on module has to be earlier than that on carrier board.

The boot up of module depends on when you release the reset signal of your carrier board. The module will boot up when the reset signal on your carrier board is released. Before that, the module will not boot up. That's why designer needs to put the *RESET_IN#* in the last stage of power to serve as the "*power good*" signal of the carrier board.

The module will not boot up till the module power is ready because the carrier board hasn't released the reset signal yet.

The sequence is as follows:

Module Power Ready --> *CARRIER_POWER_ON* -->*RESET_IN#* -->Boot Up

4.1.5. RESET_IN#

The *SMARC* module does not know the IO power status from the carrier board, and put *RESET_IN#* in the last stage of power can serve as the "*power good*" signal of carrier board. This also assures that the power of carrier board is good when *SMARC* module booting up.

4.1.6. VDD_IO

The 3.3V *VDD_IO* is depreciated from *SMARC* 1.1 specification.

SMARC-iMX93 supports 1.8V *VDD_IO* only.

4.1.7. Power Bad Indication (VIN_PWR_BAD#)

Power bad indication is from carrier board and is an input signal for Module. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) will not be enabled while this signal is held low by the Carrier.

This signal has a 100K pull-up on module and is driven by *OD* part on Carrier.

4.1.8. System Power Domains

It is useful to describe an *SMARC* system as being divided into a hierarchy of three power domains:

1) Battery Charger power domain (can be neglected if the system is not battery powered only)

2) *SMARC* Module power domain

3) Carrier Circuits power domain

The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits may include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.

The *SMARC* Module domain includes the *SMARC* module.

The Carrier Circuits domain includes “everything else” (and does not include items from the Battery Charger and Module domain, even though they may be mounted on the Carrier).

This is illustrated in the figure below.

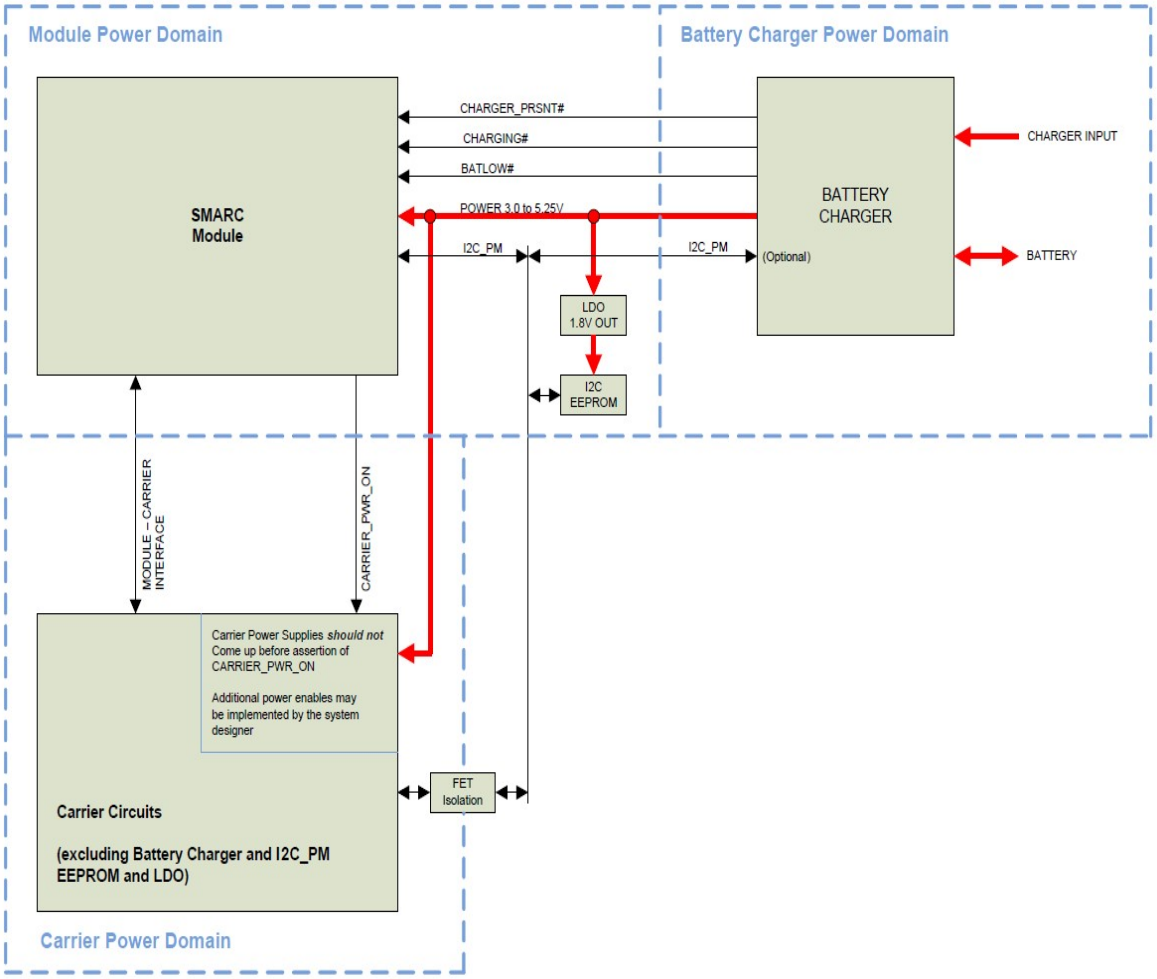


Figure 24 System Power Domains

4.2 Power Signals

4.2.1. Power Supply Signals

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
P147, P148, P149, P150, P151,P152, P153, P154, P155, P156	VDD_IN	I	PWR	3.0V~5.25V[1]	Main power supply input for the module
P2, S3, P9, S10, P12, S13, P15, S16, P18, S25, P32, S34, P38, S47, P47, P50, P53, P59, S61, S64, S67, P68, S70, S73, P79, S80, P82, S83, P85, S86, P88, S89, P91, S92, P94, P97, P100, S101, P103, S110, S119, P120, S124, S130, P133, S136, P142, S143, S158	GND	I	PWR		Common signal and power ground
S147	VDD_ RTC	I	PWR	3.3V	RTC supply, can be left unconnected if internal RTC is not used

4.2.2. Power Control Signals

The input pins listed in the following table are all active low and are meant to be driven by *OD* (open drain) devices on the Carrier. The Carrier either floats the line or drives it to *GND*. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design, and may be 3.3V or *VDD_IN*.

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
S150	VIN_PWR_BAD#	I	CMOS	VDD_IN	Power bad indication from Carrier board
S154	CARRIER_PWR_ON	O	CMOS	VDD_IO	Signal to inform Carrier board circuits being powered up
P126	RESET_OUT#	O	CMOS	VDD_IO	General purpose reset output to Carrier board.
P127	RESET_IN#	I	CMOS	VDD_IO	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.
P128	POWER_BTN#	I	CMOS	VDD_IO	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.

4.2.3. Power Management Signals

The pins listed in the following table are related to power management. They will be used in a battery-operated system.

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
S156	BATLOW#	I	CMOS	VDD_IO	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.
S154	CARRIER_PWR_ON	O	CMOS	VDD_IO	Signal to inform Carrier board circuits being powered up
S153	CARRIER_STBY#	O	CMOS	VDD_IO	Module will drive this signal low when the system is in a standby power state
S152	CHARGER_PRSNT#	I	CMOS	VDD_IO	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
S151	CHARGING#	I	Strap	VDD_IO	Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.
S149	SLEEP#	I	CMOS	VDD_IO	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.
S148	LID#	I	CMOS	VDD_IO	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.

4.2.4. Special Control Signals (TEST#)

SMARC-iMX93 does not support to boot up from *SPI NOR* flash. *SMARC-iMX93* module boots up from the onboard *eMMC* Flash first. The firmware in the *eMMC* flash will read the *BOOT_SEL* configuration and decides where to load the u-boot.

In some situations like the firmware in *eMMC* flash needed to be upgrade/restore or at factory default where the firmware in *eMMC* flash is empty or at development stage that the firmware in *eMMC* needs to be modified, users will need an alternative way to boot up from SD card first. The *TEST#* pin serves as this purpose. The *TEST#* pin is pulled high on module. If carrier board leaves this pin floating or pulls high, the module will boot up from on-module *eMMC*. If carrier board pulls this pin to *GND*, the module will boot up from *SD* card first. The first stage bootloader in *i.MX93* CPU ROM codes will load the 2nd stage bootloader based on the setting of this *#TEST* pin (*S157*).

4.3 Power Flow and Control Signals Block Diagram

Following figures shows the power flow and control signals block diagram.

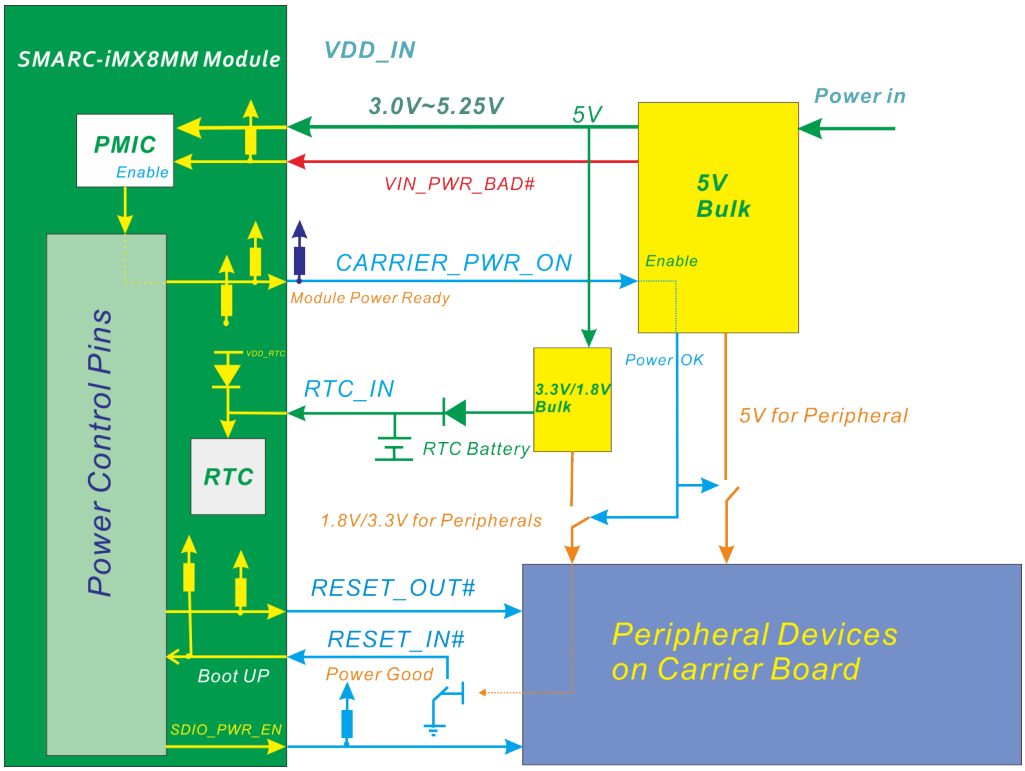


Figure 25 Power Block Diagram

When main power is supplied from the carrier, a voltage detector will assert *VIN_PWR_BAD#* signal to tell the module and carrier that the power is good. This signal will turn on the *PMIC* on module to power on the module.

Carrier power circuits in the carrier Power domain should not power up unless the module asserts *CARRIER_PWR_ON*. The module signal *CARRIER_PWR_ON* exists to ensure that the module is powered before the main body of carrier circuits (those outside the power and power control path on the carrier).

The main body of carrier board circuits will not be powered until the module asserts the *CARRIER_PWR_ON* signal being correct. Module hardware will assert *CARRIER_PWR_ON* when all power supplies necessary for module booting are ready. The module will continue to assert signal *RESET_OUT#* after the release of *CARRIER_PWR_ON*, for a period sufficient to allow carrier power circuits to come up. When Carrier power is ready, it will assert *RESET_IN#* to inform module booting up.

If users would like to have SD boot up, *SDIO_PWR_EN* signal have to be pull up to 3.3V on carrier.

Module and carrier power supplies will not be enabled if the *VIN_PWR_BAD#* is held low by carrier. It is a power bad indication signal from carrier and is 200k pull up to *VDD_IN* on module.

4.4 Power States

The *SMARC-iMX93* module supports different power states. The table below describes the behavior in the different states and which power rails and peripherals are active. Additional power states can be implemented if required using available GPIOs to control additional power domains and peripherals.

Abbr.	Name	Description	Module	Carrier Board
UPG	Unplugged	No power is applied to the system, except the RTC battery might be available	No main VDD_IN applied from fixed DC supply, VDD_IN available if backup battery is implemented	No power supply input, RTC battery maybe inserted
OFF	off	System is off, but the carrier board input supply is available	The main VDD_IN is available, but the CPU and peripherals are not running. Only the PMIC is running	Carrier board provides power for module, the peripheral supplies are not available
SUS	Suspend	System is suspended and waits for wakeup sources to trigger	CPU is suspended, wakeup capable peripherals are running while others might be switched off	Power rails are available on carrier board, peripherals might be stopped by software
RUN	Running	System is running	All power rails are available, CPU and peripherals are running	All power rails are available, peripherals are running
RST	Reset	System is put in reset state by holding RESET_IN# is low	All power rails are available, CPU and peripherals are in reset state	All power rails are available, peripherals are in reset state

The figure below shows a sequence diagram for the different power states. The module automatically enters into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to suspend by software. There might be different wake up sources available. Consult the

datasheet for *SMARC-iMX93* module for more information about the available wakeup events.

In the running state, a shutdown request can be triggered by software. This turns off all power rails on the module and requests the carrier board to switch of the power rails for the peripherals. The module can be brought back to the running mode in two ways. The module main voltage rail (*VDD_IN*) can be removed and applied again. If needed, this could also be done with a button and a small circuit. *SMARC-iMX93* module supports being power cycled by asserting the *RESET_IN#* signal (e.g. by pressing the reset button or shunt and relief the reset jumper), please consult the associated module datasheet for more information about the support power cycle methods.

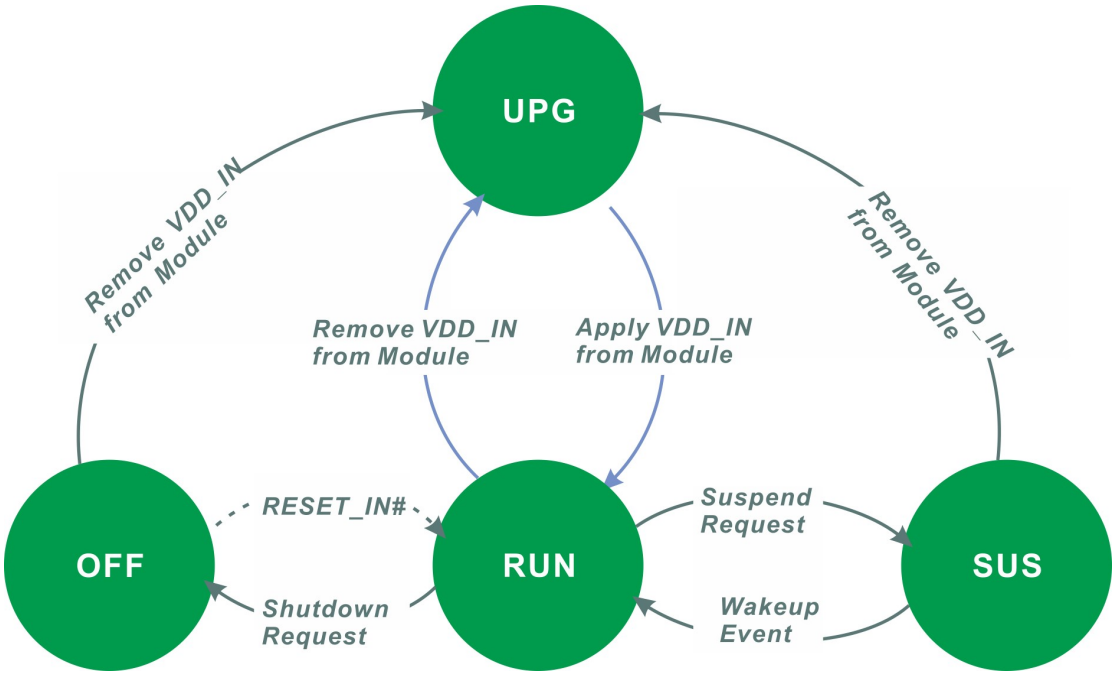


Figure 26 Power States and Transitions

4.5 Power Sequences

When main power is supplied from the carrier, a voltage detector will assert *VIN_PWR_BAD#* signal to tell the module and carrier that the power is good. This signal will enable the *PMIC* on module to power on the module. The module will not power up if the module receives a low-active *VIN_PWR_BAD#* signal.

The *SMARC-iMX93* module starts asserting *CARRIER_PWR_ON* as soon as the main voltage supply being applied to the module and all power supplies necessary for module booting are up. This is to ensure that the module is powered before the main body of carrier circuits (those outside the power and power control path on the carrier). The module will continue to assert signal *RESET_OUT#* after the release of *CARRIER_PWR_ON*, for a period sufficient time (at least 10ms) to allow carrier power circuits that the peripheral supplies need to ramp up.

The peripheral power rails on the carrier board need to ramp up in a correct sequence. The sequence starts normally with the highest voltage (e.g. 5V) followed by the lower voltages (e.g. 3.3V then 1.8V and so on). Peripherals normally require that a lower voltage rails is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for a proper sequencing. The *SMARC-iMX93* modules guarantees to apply the reset output *RESET_OUT#* not earlier than 100ms after the *CARRIER_PWR_ON* goes high. This gives the carrier board a sufficient time for ramping up all power rails. *SDIO_PWR_EN* signal have to be pull up to 3.3V on carrier if users would like to have SD boot up functionality.

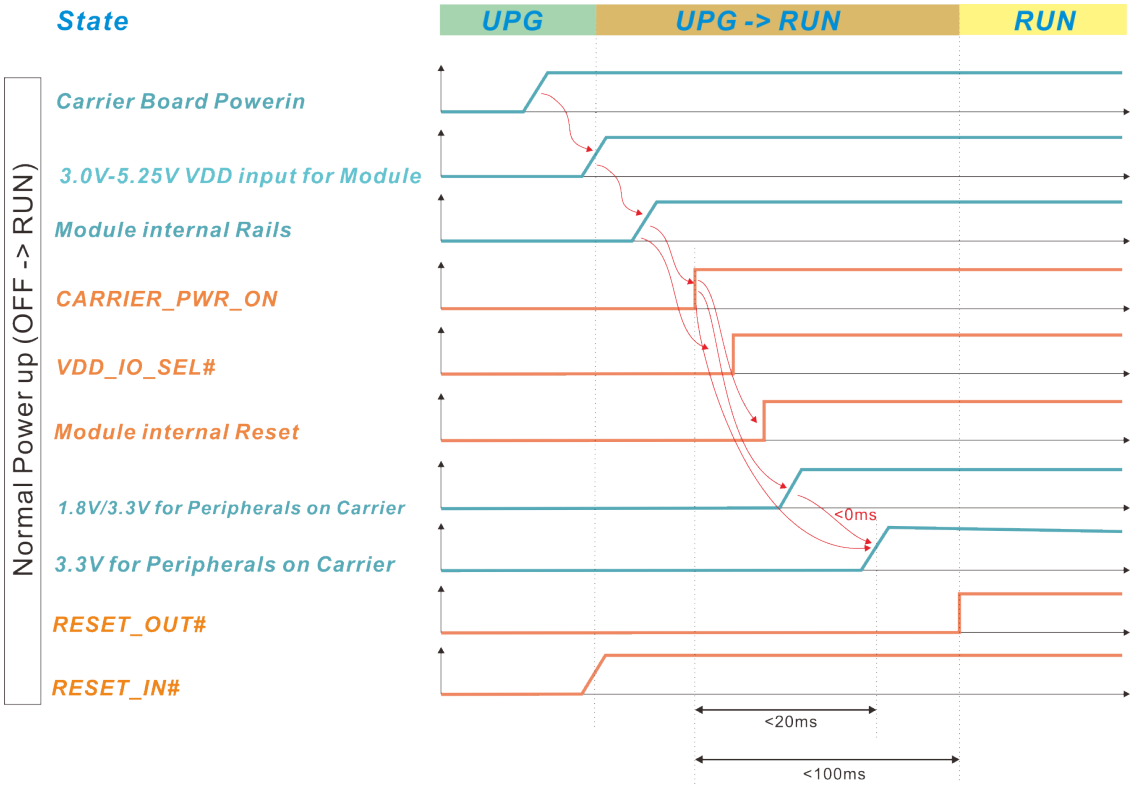


Figure 27 Power-Up Sequences

If the operating system supports it, a shutdown sequence can be initiated. Some systems may benefit from shutting down instead of just removing the main power supply as this allows the operating system to take care of any housekeeping (e.g. bringing mass storage devices to a controlled halt). Some operating system may not provide the shutdown function.

As it is not permitted that a lower voltage rail is present when a higher voltage rail has been switched off, the sequence of shutting down the peripheral voltages needs to be considered. The lower voltages (e.g. peripheral 3.3V) need to ramp down before the higher ones do (e.g. peripheral 5V).

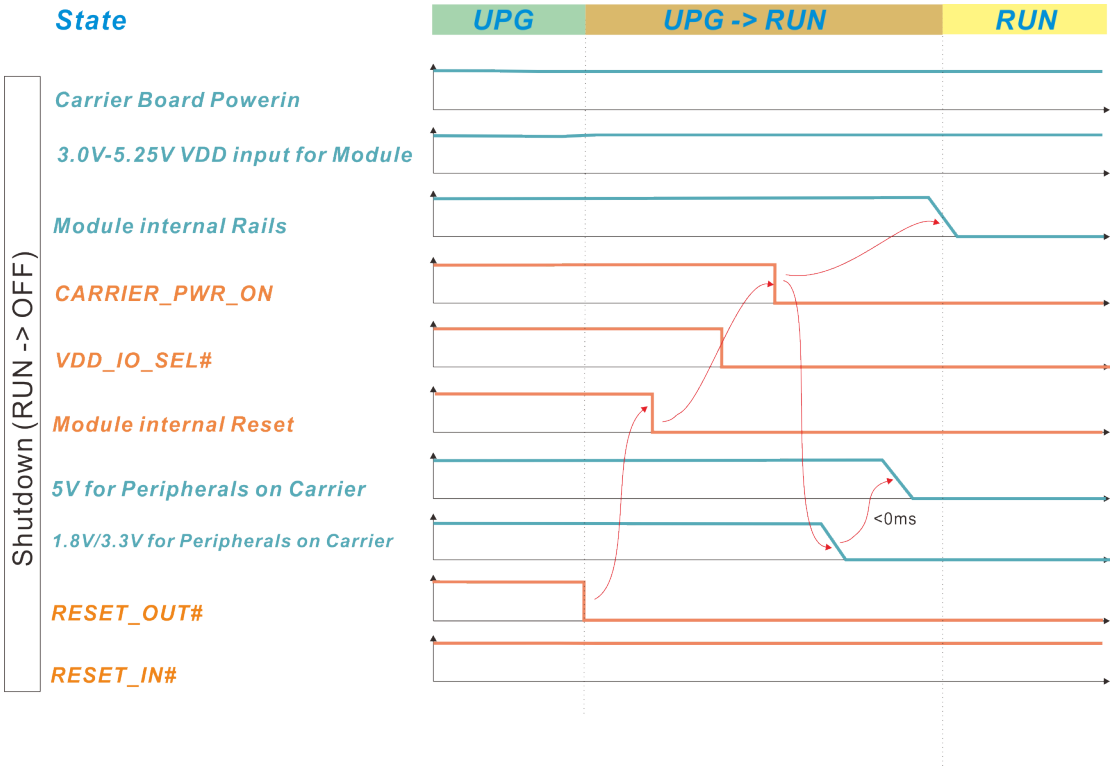


Figure 28 Shutdown Sequence

When the *RESET_IN#* is asserted, a reset cycle is initiated. The module internal reset and the external reset output *RESET_OUT#* are asserted as long as *RESET_IN#* is asserted. If the reset input *RESET_IN#* is de-asserted, the internal reset and the *RESET_OUT#* will remain low for at least 1ms until they are also de-asserted and the module starts booting again. This guarantees a minimum reset time of 1ms even if the reset input *RESET_IN#* is triggered for a short time.

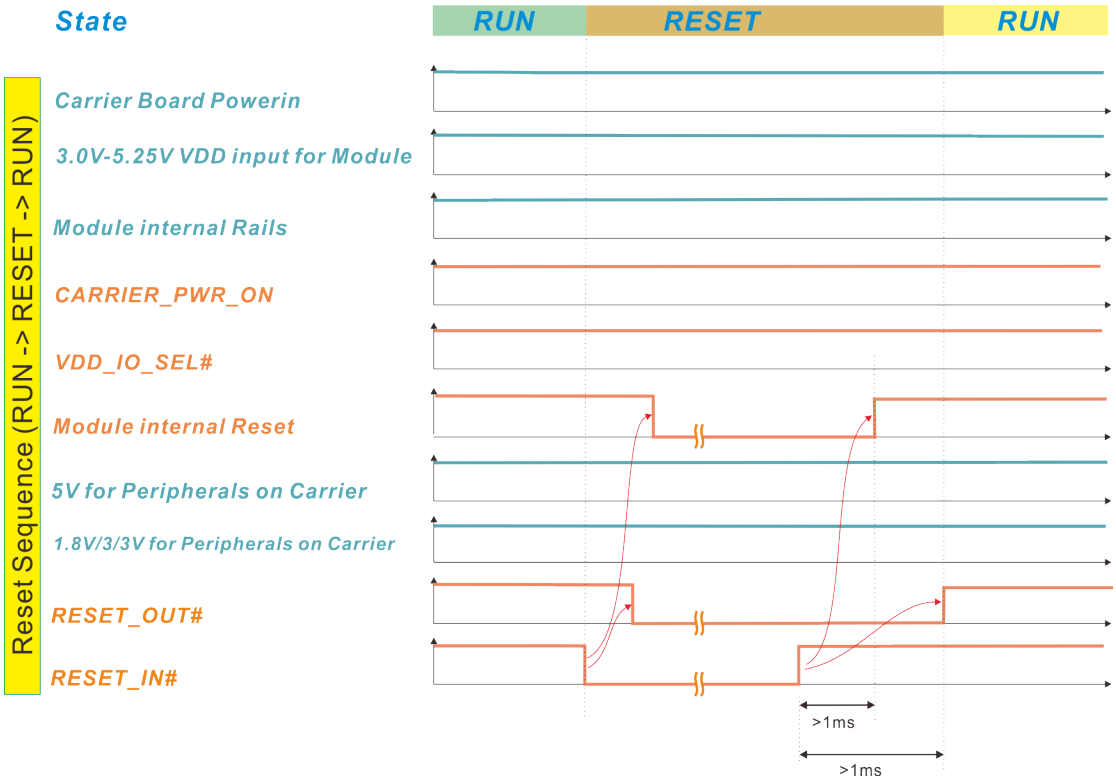


Figure 29 Reset Sequence

4.6 Terminations

4.6.1. Module Terminations

The Module signals listed below will be terminated on the Module. The terminations follow the guidance given in the table below.

Signal Name	Series Termination	Parallel Termination	Notes
I2C_PM_DAT		2.2K pull-up to 1.8V	
I2C_PM_CK		2.2K pull-up to 1.8V	
I2C_LCD_DAT		2.2K pull-up to 1.8V	
I2C_LCD_CK		2.2K pull-up to 1.8V	
I2C_CAM[0:1]_DAT		2.2K pull-up to 1.8V	
I2C_CAM[0:1]_CK		2.2K pull-up to 1.8V	
I2C_GP_DAT		2.2K pull-up to 1.8V	
I2C_GP_CK		2.2K pull-up to 1.8V	
SDIO_CD#		10k pull-up to 3.3V	
SDIO_WP		10k pull-up to 3.3V	

Signal Name	Series Termination	Parallel Termination	Notes
USB[0:4]_EN_OC#		10K pull-up to 3.3V or a switched 3.3V on the Module	x is '0' or '1' Switched 3.3V: if a USB channel is not used, then the USBx_EN_OC# pull-up rail may be held at GND to prevent leakage currents.
VIN_PWR_BAD#		200k pull-up to VIN	

4.6.2. Carrier/Off-Module Terminations

The following Carrier terminations are required, if the relevant interface is used. If unused, the *SMARC* Module pins may be left un-connected.

Module Signal Group Name	Carrier Series Termination	Carrier Parallel Termination	Notes
GBE_MDI	Magnetics module appropriate for 10/100/1000 GBE transceivers	Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	
GBE_LINK **(GBE status LED sinks)**		If used, current limiting resistors and diodes to pulled to a positive supply rail	The open drain GBE status signals, GBE_LINK100#, GBE_LINK1000# and GBE_LINK_ACT#, if used, need Carrier based current limiting resistors and LEDs. The LED may be integrated into a Carrier RJ45 jack. A resistor of 68 ohms, and a LED with the anode tied to Carrier 3.3V, is typical.
LVDS LCD		100 ohm resistive termination across the differential pairs at the endpoint of the signal path, usually on the display assembly	

4.7 Boot Device Selection

SMARC hardware specification defines three pins (*BOOT_SEL[0:2]*) that allow the Carrier board user to select from eight possible boot devices. *SMARC-iMX93* does not support boot up from SPI flash. If *TEST#* is not shunt cross to GND, the first stage of bootloader on *SMARC-iMX93* will boot up from on-module *eMMC* first. The firmware on *eMMC* will read the boot device configuration and load the second stage bootloader from selected boot devices. The *BOOT_SELx#* pins are weakly pulled up on the Module and the pin states decoded by module logic. The Carrier shall either leave the Module pin Not Connected ("Float" in the table below) or shall pull the pin to GND, per the table below.

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI
4	Float	GND	GND	Module Device (USB)
5	Float	GND	Float	Remote Boot (GBE)
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

If *TEST#* pin is shunt cross to GND, the first stage of bootloader on *SMARC-iMX93* will boot up from off-module *SD* card. This is a back door to restore/upgrade the firmware in on-module *eMMC*.